Hardware Digital Protection

by

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A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

October, 1979

Order Number 1355688

Hardware digital protection

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King Fahd University of Petroleum and Minerals (Saudi Arabia), 1979

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DHAHRAN : SAUDI ARABIA

This thesis, written by

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MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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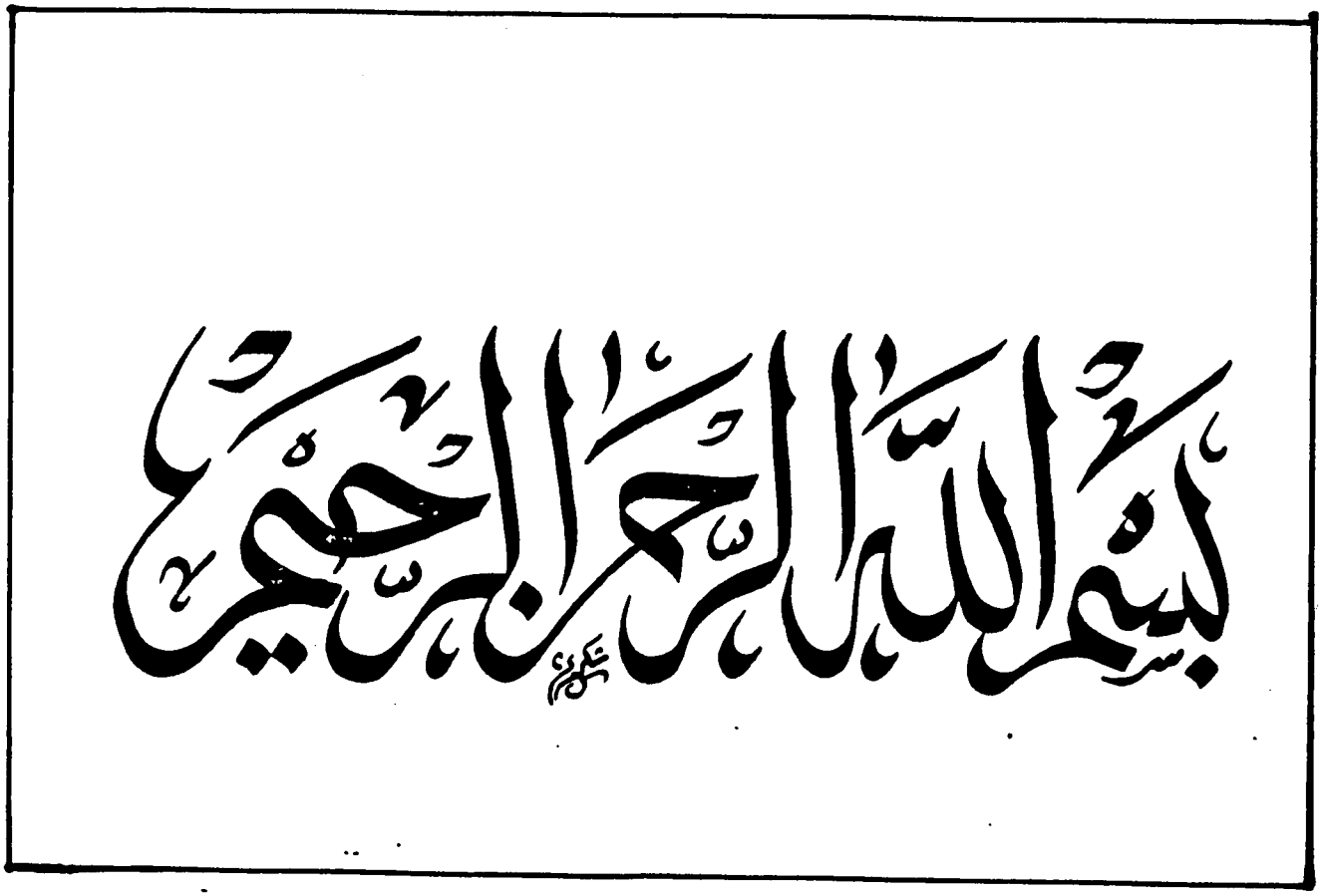
بسم الله الرحمن الرحيم

قال تعالى


فاذكروني أذكركم

This Thesis is dedicated to my dear parents.

ACKNOWLEDGEMENTS

Acknowledgement is due to the University of Petroleum and Minerals for support of the research leading to this Thesis.

I wish to express my deep appreciation to Asst. Professor Dr. Ahmed Farag who served as my major advisor. I also wish to thank the other members of my Thesis Committee, Professor Ali M. Alli and Asst. Professor Dr. Mansoor Alam.

Thanks are also to Dr. Moh'd Osman for his valuable assistance and guidance.

I would like to thank also the EE laboratory technicians and the EE Secretary Mr. Khalid Butt for their cooperation in preparing this manuscript.

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ABSTRACT

The design and construction of a prototype hardware-oriented digital overcurrent relay is presented. This newly designed digital relay is available to provide virtually all the functions traditionally associated with the existing relays for the protection of power systems and circuits against overcurrents and faults.

Experimental results on a laboratory model are presented beside the time-current characteristics of different relay models. Test performance of the digital overcurrent relay shows that such a device is feasible and offers some distinct advantages over existing devices.

By various adjustments, such a unit can operate as an Inverse, Very Inverse, Extremely Inverse, Short-time, Long-time, and Definite-time Overcurrent relays.

INTRODUCTION

Protection in an electric system is a form of insurance. It pays nothing as long as there is no fault or other emergency, but when a fault occurs it can be credited with reducing the extent and duration of the interruption, the hazards of property damage and personnel injury. Every system is subject to short circuits and grounds that should be removed quickly by designing suitable relay protection.

The work presented in this thesis forms a project devoted to the development of integrated and compatible digital overcurrent relay. The development, construction and testing of a new hardware digital overcurrent relay is thoroughly investigated.

Chapter 1 describes the causes of faults, their types, zones of protection, the progress in the development of relays and protective schemes, the recent advances in digital technology and the developments in digital protection.

The description of different types of protective relays and their performance is discussed in chapter 2.

In chapter 3, the prototype of a hardware - oriented digital overcurrent relay is depicted. The device is designed and built to test the basic principles involved. Many of the features suggested for the overall digital overcurrent relay are accommodated.

Different experimental results on the laboratory model are presented in chapter 4. Also discussions and comparisons between the digital hardware relay with conventional relays are presented.

Chapter 5 provides all possible modification circuits that can be implemented on the digital overcurrent relay.

Chapter 6 draws conclusions concerning the results achieved throughout the thesis and gives suggestions for future research.

1. PROTECTION

Industrial plants vary greatly in the complexity of their electric systems; the smallest having only a small radial system with fuse protection, and the largest having an intricate combination of buses, lines, and circuit breakers requiring very complete relay protection. While most industrial users purchase all of their electric energy, there are many who generate part or all of their requirements, sometimes operating in parallel with local utility generation. Invariably the local utility requires fault protection at the service entrance to the industrial plant, and in all cases at an early stage of design, the engineer should consult with the utility regarding fault protection requirements |1,2|.

The primary objective of an industrial plant is to produce consistently and economically. The ability to produce is dependent on the adequacy and continuity of the electric service, and service interruptions can be evaluated directly in terms of lost production. Usually, the cost of loss of lost production exceeds the cost of physical damage to equipment involved in a fault. Therefore it is important to the industrial operation that the electric system be properly designed so that protective equipment can be applied in such a manner as to isolate faults quickly and with a minimum of service interruption |1-3|.

In addition to production loss, system faults can result in injury to personnel and extensive property damage either directly or as a result of a fire or explosion. Also, a serious uncleared fault in a plant can jeopardize the utility operation and result in an area outage that would affect numerous other customers. These basic factors including production loss, personnel injury, property damage, and consideration for other users of the service should be included together with the engineering requirements in determining the fault protection that is required |1,2,4|.

The losses associated with a service interruption vary widely in different types of industries. For example, a service interruption in a machine operation may mean only a delay in production, while a similar interruption in a chemical reduction plant can cause loss of material and production, costly cleanup operations and possible damage to production equipment. Other industries such as refineries, paper mills, textile mills, and processing plant are affected similarly, but in varying degrees. For some types of loads, such as paper, film, textile fibre processes, and others involving complex automation, a momentary voltage dip can be as serious as a complete interruption. Others can tolerate a momentary interruption, but not a sustained one. *Thus, the relay of industrial operation has a major influence on the type of fault protection applied to the electric system* |2,3|.

Some industrial plants, because of their size or the nature of their operations, are able to maintain electrical engineering

staffs capable of the design, installation and maintenance of an efficient protective system; while others will probably find it is more economical to engage competent engineering advice and services from consultants. This work is specialized and often very complex, and it is neither safe nor fair to the operating engineer to expect him to do it as a sideline. Neither it is feasible for the equipment manufacturer or the local utility to maintain a sufficient force to provide this service |1-7|.

1.1 PROTECTION AND ITS PURPOSE

The capital investment involved in a power system for generation, transmission, and distribution of electrical power is so great that the proper precautions must be taken to ensure that the equipment not only operates as nearly as possible to peak efficiency, but also that it is protected from accidents.

The normal path of electric current is from the power source through copper (or aluminium) conductors in the generators, transformers and transmission lines to the load and it is confined to this path by insulation |2-4|.

Every system is subjected to short circuits and grounds that should be removed quickly. Protection in an electric system is a form of insurance. It pays nothing as long as there is no fault or other emergency, but when a fault occurs it can be

credited with reducing the extent and duration of the interruption, the hazards of property damage and personnel injury. It would be ideal if protection could anticipate and prevent faults but this is obviously impossible except where the original cause of a fault creates some effect which can operate a protective relay. So far only one type of relay falls within this category; this is the gas detector relay, used to protect transformers, which operates when the oil level in the conservator pipe of a transformer is lowered by the accumulation of gas caused by a poor connection or by an incipient breakdown of insulation. With all other equipment it is only possible to mitigate the effects of a short circuit by disconnecting the equipment as quickly as possible, so that the destructive effects of the energy into the fault may be minimized |2|.

1.2 CAUSES OF FAULTS AND THEIR TYPES

It would be neither practical nor economical to build a fault-proof power system. Consequently, modern systems are designed with reasonable precautions to provide sufficient insulation, clearances, etc. but a certain number of faults must be tolerated during the life of the system. Even with the best design possible, materials tend to deteriorate and the likelihood of faults increases with age |1,2,8,9|.

Insulation is usually air or a high resistivity material which may also be used as a mechanical support. Air insulation can be accidentally short-circuited by birds, rodents, snakes, kite-strings, tree limbs, etc., or reduced in insulation strength by ionization due to lightning or a fire. Organic insulation can deteriorate due to heat or ageing, or can be broken down by over-voltage due to lightning, switching surges, etc. Porcelain insulators can be bridged by moisture with dirt or salt and become cracked. In all these cases the initial lowering of insulation resistance causes a small current to be diverted which hastens deterioration or ionisation, causing this current to increase in a progressive manner until a power arc occurs. Furthermore, heavy faults, if not quickly interrupted, may heat conductors sufficiently to cause deterioration of other insulation which was previously in healthy state.

Line and apparatus insulation may be subjected to transient overvoltages whenever current is started or stopped. These surges are a component of the "recovery" voltages and are analogous to "water hammer" when a hydraulic valve is suddenly closed |2,5,6|.

The ordinary types of faults that protective relays must detect are three-phase, phase-to-phase, two-phase-to-ground, and single-phase-to-ground short circuits |1|.

1.3 ZONES OF PROTECTION

The general philosophy of relay application is to divide the power system into protective zones that can be protected adequately with a minimum amount of the system disconnected. The power system is divided into protective zones for:

1) Generators.
2) Transformers.
3) Buses.
4) Transmission and distribution circuits.
5) Motors.

A typical power system and its zones of protection are shown in Fig. 1.1. The purpose of the protective system is to provide the first line of protection. Since failures do occur, however, some form of backup protection is provided to trip out the adjacent breakers or zones surrounding the trouble area.

Protection in each zone is overlapped to avoid possibility of unprotected areas. This overlap is accomplished by connecting the relays to current transformers as shown in Fig. 1.2. Fig. 1.2(a) shows the connections for "dead tank" breakers and Fig. 1.2(b) shows the "live tank" breakers commonly used with extra high voltage circuits. Any trouble in the small area between the current transformers will operate both Zone A and Zone B relays and trip all the breakers in the two zones. In Fig. 1.2(a), this small area

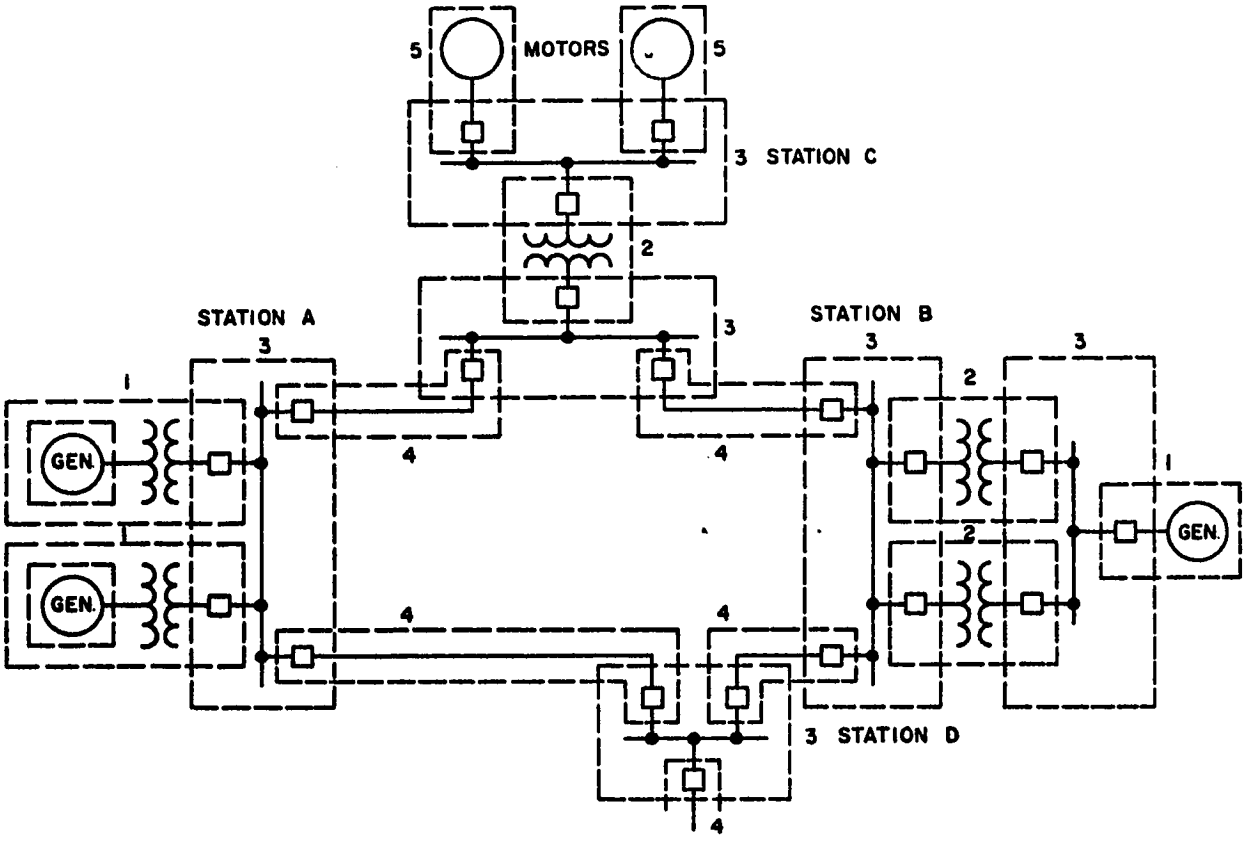
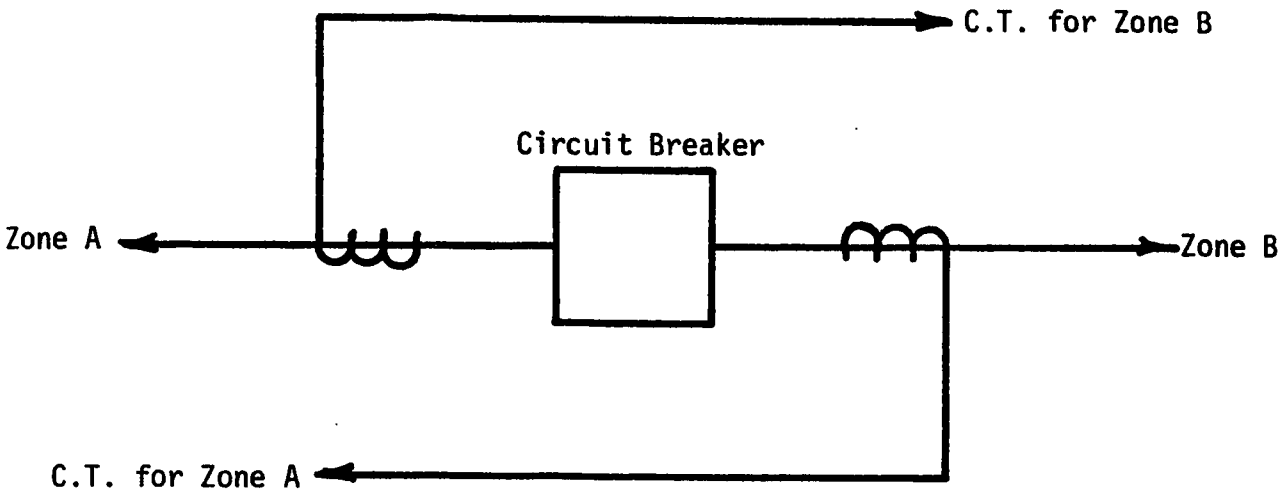
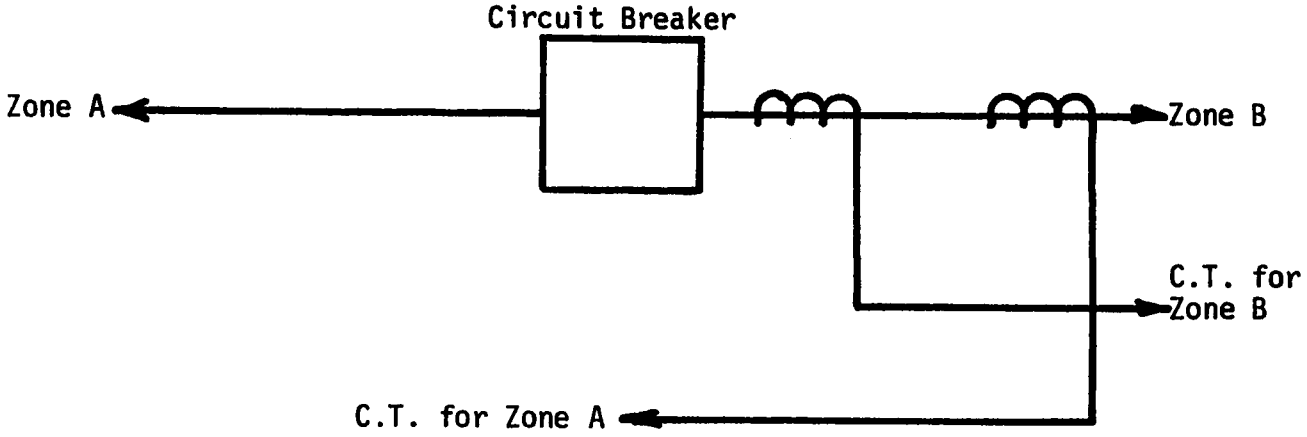


Figure 1.1. A typical system and its zones of protection.



(a). Dead Tank Breaker and Breakers With Separate Current Transformers on Both Sides of Breakers.



(b). Live Tank and Breakers with a Separate Current Transformers on one side only.

Figure 1.2. The Principle of Overlapping Protection Around a Circuit Breaker.

represents the breaker and, in Fig. 1.2(b), the current transformer, which may or may not be part of the breaker |3|.

1.4 TYPES OF PROTECTION

The different types of protection are |3,4,7,10|:

1) Generator Protection.
2) Motor Protection.
3) Transformer Protection.
4) Station-Bus Protection.
5) Line and Circuit Protection.

1.4.1 Generator Protection:

The following kinds of protection are applied to the Generator |3,4,7,10|:

a) Ground-fault protection.
b) Back up protection.
c) Overload protection.
d) Over-speed protection.
e) Loss-of-excitation protection.
f) Protection against Generator Motoring.
g) Field Ground Protection.
h) Alternating-Current Overvoltage Protection for Hydroelectric generators.
i) Generator Protection at Reduced Frequencies.

1.4.2 Motor Protection:

The Motor has the following kinds of protection which can be applied to it |3,4,7,10|:

a) Phase-fault Protection.

b) Ground-Fault Protection.

c) Locked-Rotor Protection

d) Overload Protection

e) Low Voltage Protection.

f) Phase-Rotation Protection.

g) Phase-Unbalance Protection.

h) Out-of-step Protection.

i) Loss of Excitation.

1.4.3 Transformer Protection:

The following kinds of protection can be used for the transformer protection |3,4,7,10|:

a) Differential Protection.

b) Protection of Phase-Angle Regulator and Voltage Regulators.

c) Zig-zag transformer Protection.

d) Interconnected, Wye-Delta Transformer Protection.

e) Protection of Shunt Reactors.

1.4.4 Station-Bus Protection:

This type of protection can have the following kinds of protection |3,4,7,10|:

a) The Linear Coupler Differential Protective System.

b) Multi-Restraint Differential Protective System.

c) High-Impedance Differential Protective System.

d) Protecting a Bus that Includes a Transform Bank.

e) Other Bus-Protective Schemes such as:

1. Overcurrent-Differential Relaying.
2. Partial-Differential Relaying.
3. Directional-Comparison Relaying.
4. Fault Bus (Ground Fault Protection).

1.4.5 Line and Circuit Protection:

The following kinds of protection are applied |3,4,7,10|:

a) Distribution Circuit Protection.

b) Subtransmission Circuit Protection.

c) Transmission Circuit Protection.

d) Ground Fault Protection.

e) Series Compensated Transmission Line Protection.

1.5 PROGRESS IN THE DEVELOPMENT OF RELAYS AND PROTECTIVE SCHEMES

In the very early days of the electrical industry, a power system usually consists of a small generator supplying a local load

and it was possible for the station attendant, in an emergency case, to open a switch manually and even swat out the arc with a duster. Since these historic times the sizes of power systems have increased enormously, the rate of increase for most countries laying between a doubling and a quadrupling per decade. Furthermore, industrialised countries and an increasing number of under-developed ones have integrated their systems on a national basis and numerous cases of substantial international connections are in evidence. With increases in the sizes of a generating plant and inter-connection, great demands have been made on the ingenuity of the designers of automatic switchgear. Such apparatus must operate to interrupt very high arc energies in a small fraction of a second if the equipment is to be safeguarded.

Fuses were the first automatic devices to be employed to isolate the faulted equipment quickly. They were very effective and are still widely used in distribution circuits, but suffer from the disadvantage of requiring replacement before the power supply can be restored. This inconvenience was overcome by the automatic circuit breaker with a built-in overload or under-voltage trip magnet. The final step was to divorce the selective function from the breaker and to incorporate it in separate protective relays, whose contacts controlled the trip coil of the breaker |2,11,12|.

The first attempts to design relays which would operate in response to short-circuit conditions involved attracted armature

devices, with or without a definite time-delay provided by a dashpot mechanism. As power systems increased in size and complexity it was necessary to employ more precise relay mechanism and to obtain selectivity on an inverse time-current basis, i.e. the relay speed increasing with the current magnitude so that, since the current is greatest in the faulted section, that section will be isolated by its relays before those in the sound sections can operate. The only device then available which, had this required accuracy, was the induction disc watt-hour meter which was turned into a relay by substituting contacts for the indicating register. This results in the inverse time-overcurrent relay which is still in use today, although in an improved form as shown in Fig. 1.3 |2,11,12|.

As the requirements for sensitivity and selectivity increased, a trend emerged towards the use of high-speed differential type relays on the main transmission system, time-overcurrent relays being retained only for distribution systems and for back-up purposes (reserve protection) on the main system. Differential relays compare electrical quantities derived from each end of the protected system (e.g. a 10 miles transmission line) and operation takes place if the ratio, phase angle or algebraic sum of the derived quantities depart by a predetermined amount from some initially set value, for example, unity in the case of a differential relay measuring numerical ratio |2,11,12|.

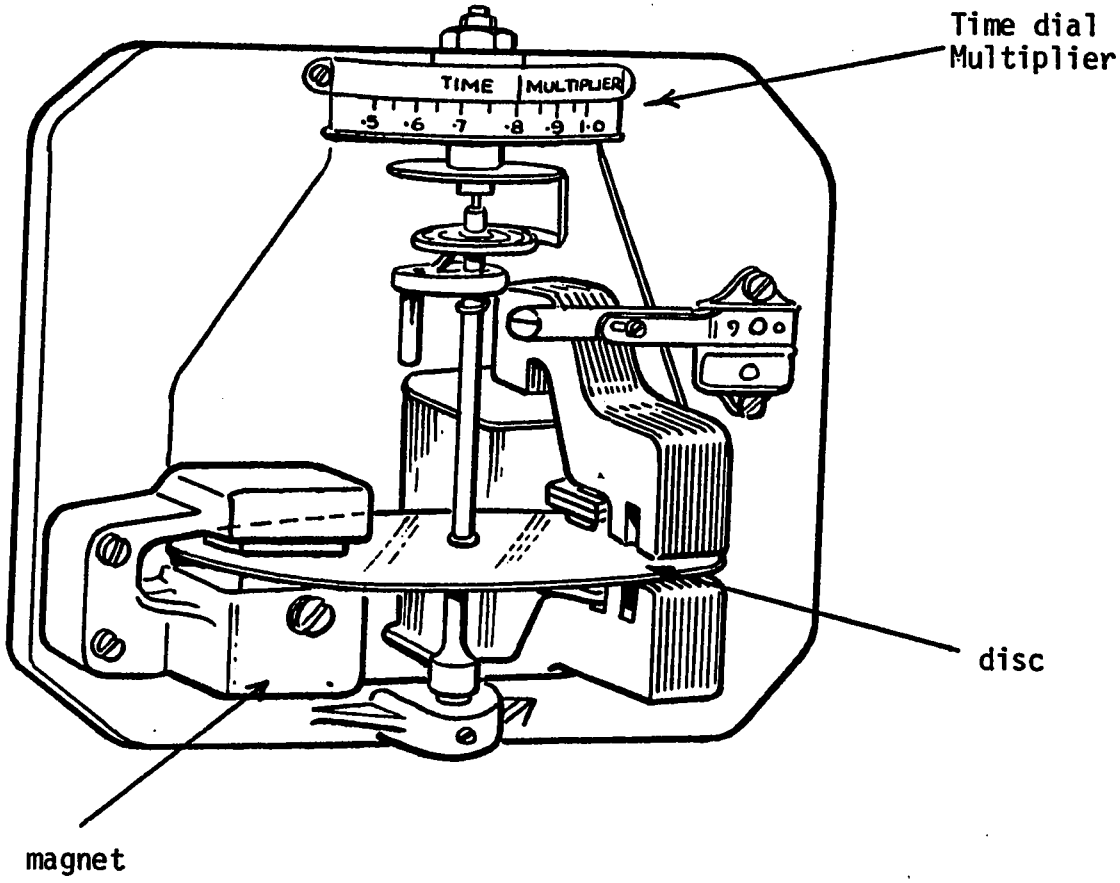
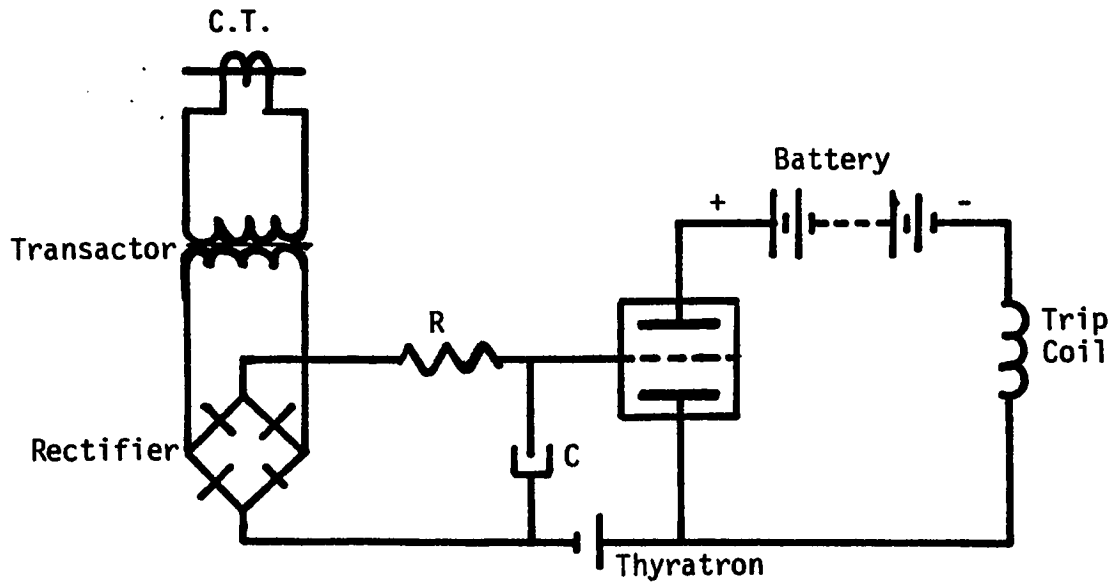


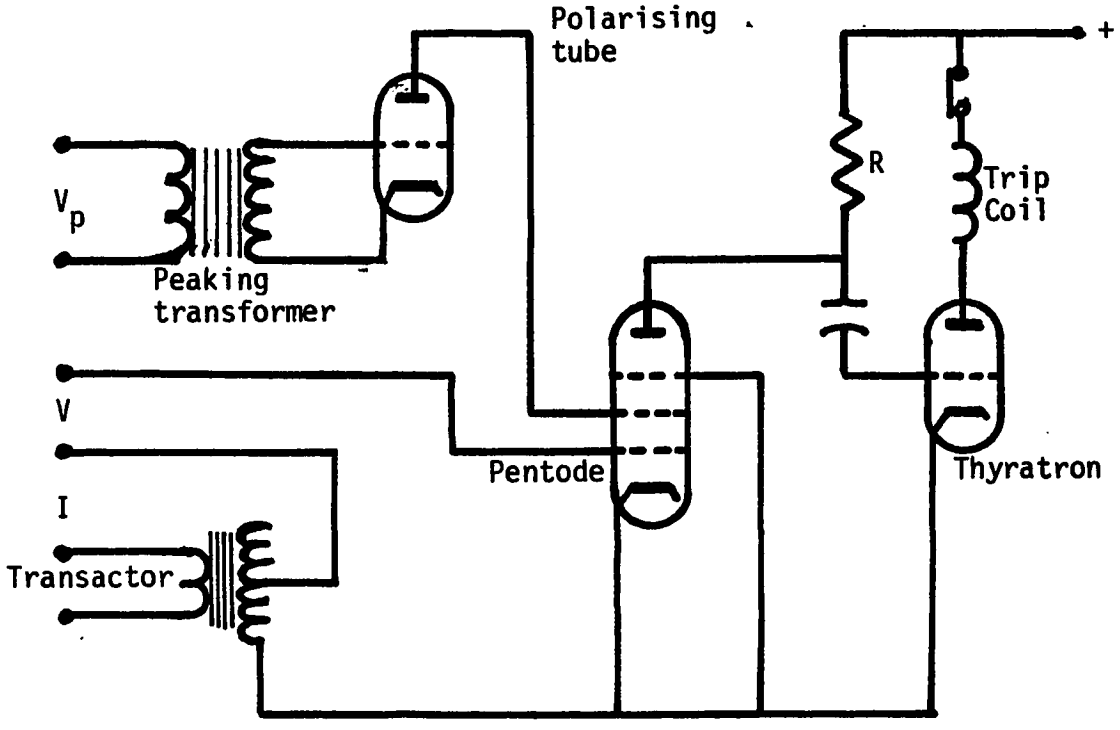
Figure 1.3. Modern Induction Disc Relay.

The induction disc inverse time relay was introduced in the early 1920's and the high-speed differential type in the late 1920's. Initially, the differential type also employed the induction disc principle but with short contact travel and a lighter armature. The desire for high speed led to the balanced beam unit but this was gradually displaced by the induction cup, which was a faster version of the induction disc unit, its inertia having been reduced by forming the disc into a narrow cup and its torque increased by better utilization of the available flux in a 4-pole magnetic structure similar to that of an induction motor. Greater sensitivity and accuracy have been achieved, particularly since the 1939-45 War, by the use of polarized d.c. relays energised through rectifier bridges |2,11,12|.

The high ratings of the relays based on electronic valves arises from the form of assessment adopted, and should not overshadow the fact that these relays have failed, over a period of 30 years, to obtain acceptance in the power industry. This is not withstanding the absence of contacts or bearings, with ensuring ease of maintenance and very fast operation, even when close to pick-up level. The reasons for non-acceptance are not hard to find; in spite of a number of excellent operating features these relays failed, other than for special purposes, on grounds of complexity and the short life of vacuum tubes. The basic arrangement of two electronic relays are shown in Fig. 1.4 |2,11,12|.



(a) Time-overcurrent relay



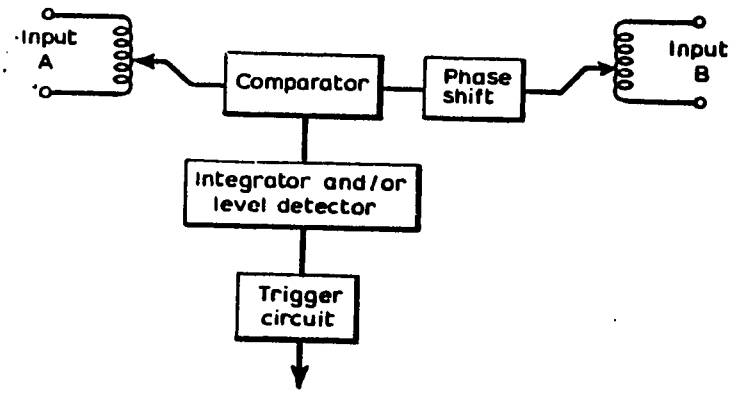
(b) Mho relay based on a pentode

Figure 1.4. Electronic Relay Units.

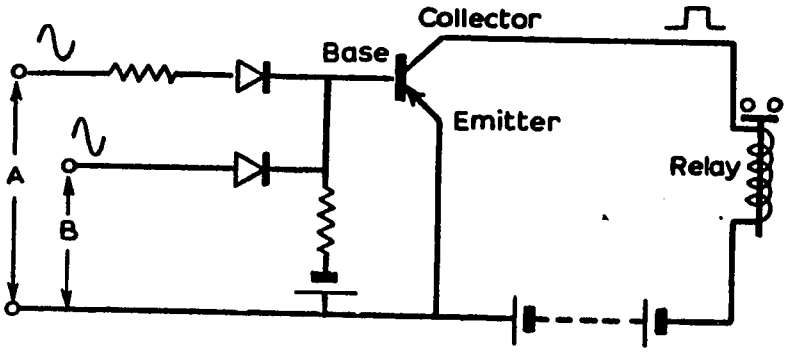
Transistor relays are being developed by several large electrical manufacturers. They appear to have the advantage of electronic relays based on thermionics, without their disadvantages. The earlier transistor relays were using transistors only as switches or amplifiers, so that changes in their characteristics due to temperature or ageing will not affect relay calibration. Transistor relays are smaller, cheaper, and faster than electromagnetic relays. In addition, their high sensitivity permits much smaller current transformers to be used and more sophisticated characteristics to be obtained.

The first use of transistors in protective relaying was in the field of carrier protection. Two elementary arrangements of relays, based on transistor comparators, are shown in Fig. 1.5(a,b) (Transistor comparators are used as relays) |2,11,12|.

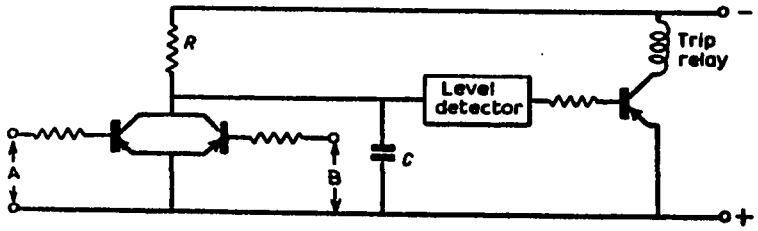
In electronic relays, the movement is replaced by electronic components and circuitry. In amplitude comparators, the two a.c. quantities, to be compared, are rectified and applied in opposition in the control grid circuit of an electronic tube, so that the operation occurs when one quantity exceeds the other by an amount depending on the bias. In phase comparison circuits, one a.c. quantity can be connected to the control grid of an electronic tube and the other a.c. quantity to the screen grid of the tube as in Fig. 1.4(b). Operation occurs when the two quantities are in phase. The reliability of this class of equipment is dependent on the quality of the components and their connections.



(a) Block diagram of static relay



(b) Multiple inputs to transistor base



(c) Inputs to matched transistors

Figure 1.5. Transistor comparators used as relays.

The main drawbacks of electronics based on thermionic tubes are:

1) Constant drain of the station battery for heater supply.
2) The provision of a minimum d.c. voltage of 120V, for plate (anode) circuits, which necessitates a battery voltage of 180V at least to allow for negative grid bias supplied and a suitable margin for voltage drop during the closing of a circuit breaker.
3) The relays in use in the greatest quantities, such as time-overcurrent relays, are more complicated in electronic design than their electromagnetic counterparts; the basic arrangement is shown in Fig. 1.4(a).
4) Limited output capacity which necessitates a mechanical relay for tripping the circuit breaker.
5) Uncertain life of the electronic tubes.

Transistor relays have similar limitations. Items 3 and 4 above apply directly.

The circuitry of transistors has some similarity to that of electronic tubes; those at present available differ in having low input impedance and are current-fed devices. A phase comparator can be made either by connecting two transistors back-to-back as in Fig. 1.5(c) or by applying the input signals in

parallel through diodes as shown in Fig. 1.5(b), so that the transistors acts as an "AND" device causing the transistor to cut-off if either of the input quantities is positive.

In either of the above circuits, current of constant magnitude will flow in the collector circuit only when the input a.c. quantities are simulataneously negative; a relay in the collector circuit will pick up when the overlap angle exceeds a certain value, i.e. when the mean d.c. level in the collector circuit exceeds the relay pick-up level as a result of phase coincidence |2,11,12|.

Solid-state relays are now available to provide virtually all of the functions traditionally associated with the protection of medium voltage circuits. This new technology allows manufacturers to take a new look at some old problems, and take advantage of improved performance characteristics |13|.

With solid-state design techniques at their disposal, modern relay designers are able to over-come previous design limitations so that they need not longer be content with system protection that is limited by the relay design, but rather, choose relays which are designed to provide the protective function |13|.

With the increase in power network capacity and voltage, a need for protection systems which clear faults very rapidly has arisen. Many schemes using digital and logic techniques are being developed. In the past, electromagnetic relays have provided excellent power system protection. At present, relays provide the most

reliable method of protection for voltages up to 230 KV. However, long extra high voltage transmission lines are susceptible to faults which the electromagnetic relay cannot sense. |14|.

Continuing rapid advances in digital computer technology have prompted a re-evaluation of protective devices and techniques. A digital system to completely overlay a power system is of considerable interest since it could provide a facility to monitor, control and protect the power system on an integrated and coordinated basis.

The use of digital computers in power systems for data logging and analysis, alarm processing, contingency evaluations and economic dispatch is well established. Some work has been done on power system digital control.|15|.

1.6 RECENT ADVANCES IN DIGITAL TECHNOLOGY

During the past twenty years, there have been tremendous advances in digital technology which has resulted in market expansion and dramatic reductions in cost and increased reliability of discrete digital components and digital computers | 16 |. This in turn has stimulated widespread interest in the use of digital techniques for real-time process control using on-site and on-line digital computers linked to a multi-level computer control system.

The widespread use of computers has been directly related to their increased performance and reliability at lower costs, all made possible by better logic and memory circuits that improved technology has made available. This technology lies in two main categories, the commonly used bipolar circuitry and metal-oxide semiconductors (MOS). At present, the characteristics of MOS technology include smaller device geometry, higher density and lower power dissipation. It requires a simpler fabrication process, limited drive capability, and non-compatibility with bipolar circuitry. Slower switching speed of MOS, below that of bipolar device, leaves the area of high performance such as memory units to the bipolar device | 17|.

The evaluation of integrated circuit technology in the era of large-scale integration (LSI) has resulted in a dramatic improvement in device density which, in turn, promises decreased cost, size, weight and power dissipation, and increased reliability. LSI is most efficiently implemented in symmetrical logic |16, 17|,

such as read-write memories (RWM), read-only memories (ROM), read-mostly memories (RMM), shift registers, and holding registers.

1.7 DEVELOPMENTS IN DIGITAL PROTECTION

G.S. HOPE worked on techniques using sequential logic for power system protection. He suggested some ways in which distance protection can be achieved by:

(i) Developing a computer program for the calculation of transmission line impedance(s).

(ii) Developing a logic protection scheme using the principles of the electromagnetic relay. Sensitivity and speed however are improved by the elimination of inertia and the reduction of power requirements.

(iii) The direct implication of a sequential machine with special logic circuit developed directly for the determination of system impedance.

(iv) Developing a group of sequential machines based on the principles of the electromagnetic relay. These sequential machines would use the system or block approach to achieve the functions performed by the protection rather than a static analogy of each function in the electromagnetic device |14|.

G.D. ROCKEFELLER worked on the development of a fundamental basis for the use of a time-shared stored-program computer to perform many of the electrical power-system protective-relay functions in a substation. Logic operations were given to detect the fault, locate it and initiate the opening of the appropriate circuit breakers, whether the fault is in the station or on lines radiating from the station.

The instantaneous values of the station voltages and currents were sampled at a 0.5 m sec. rate, converted to digital form, and stored for computer main-frame use. Computer speed in initiating tripping is a maximum of 4 m sec. for severe faults and a maximum of 10 m sec. for moderate or distant faults |18|.

M.S. Sachdev and D.W. Wind worked on a real-time hybrid, analog-digital, computer technique for differential protection of generators. The fault/no fault decisions are based on the amplitude ratio of the "fault" and "average through" currents from a selected generator phase. Analog input data pre-processor, fault monitor and soft-ware segments suitable for valid comparison during the transient period after the inception of a fault were worked-out |15|.

J.G. GILBERT and R.J. SHOVLIN worked on an algorithm for calculating apparent transmission line impedance to the point of a fault, which is an approach to distance type protection via a dedicated digital computer. Phase voltages and currents were sampled asynchronously approximately 24 times per cycle and operated on to yield apparent resistances and reactances. The transmission line

impedance calculation makes use of trigonometric identities |19|.

P.K. DASH, O.P. MALIK, and G.S. HOPE worked on an on-line digital computer technique for the protection of a generator against internal asymmetrical faults. The technique relies on the detection of a second harmonic in the armature winding. The total time for internal fault detection and tripping is well within half a cycle of the 60 HZ signal. The authors have chosen a sample rate of 16 samples per cycle as a suitable compromise between conflicting issues resulting from using a low pass analog filter to limit the frequency of the input signal, to the sampler, to less than one half the sample frequency to avoid sampling errors, and the time delay introduced by the analog filter which is inversely proportional to the sample rate |20|.

G.W. SWIFT, J. MOHD-JARJIS, A.W. DeGROOT, L.M. WEDEPOHL, and N.J. MORPHY worked on generating low-power test signals for low-power-requirement electronic distance relays using a mini-computer for steady-state and dynamic testing of distance relays |21|.

B.J. MANN and I.F. MORISON worked on a digital computer program for the protection of a three-phase transmission line by detecting the presence of a disturbance, classifies the fault into one of six fault types and, using a method of impedance calculation to determine the modulus and phase of the impedance of the faulted line |22|.

B.C. WIDREVITZ and R.E. ARMINGTON worked on a digital relay for power systems application which responds to both frequency and rate of change of frequency. Its application is in the operating situation of load suddenly in excess of generation, either because of sudden unexpected added load or because of generator or other equipment failure. Its function is the initiation of preplanned emergency load shedding. The desired trip characteristic are obtained by measuring the period of two consecutive cycles, storing and calculating the difference |23|.

W.D. BREINGAN, M.M. CHEN, and T.F. GALLEN worked on a laboratory investigation of a digital system for the protection of transmission lines using a computer with its data acquisition system connected to a transmission line model. The minicomputer program, for a two-zone stepped-distance protection scheme, utilizes an algorithm based on the system differential equation. Trip times were on the average equal to or less than 0.5 cycle for the primary protection zone. The program successfully determined fault type and location |24|.

R.R. LARSON, A.J. FLECHSIG, and E.O. SCHWEITZER worked on an inrush current-detection algorithm for the protection of transformers and a differential overcurrent algorithm and implementation on a popular eight-bit microcomputer system. Multiplication and division was avoided, enabling the use of relatively low-cost processing hardware. A hardware model centered around a transformer generated current data for the data acquisition system. This system translated

the time-continuous analog data into the time-discrete digital input data for the algorithms resident in the microcomputer. The internal fault trip was initiated at a maximum of 19.1 m sec. after fault indication when inrush current was not involved |25|.

T.F. GALLEN, W.D. BREINGAN, and M.M. CHEN worked on a digital system for directional comparison relaying, with two microcomputers communicating with each other via power line carrier. The system included a directional-comparison blocking scheme with first zone high-speed tripping. A data transfer controller is used to set the sampling rate of the digitizing subsystem which is chosen as 16 samples per cycle (960 samples per second) |26|.

2. PROTECTIVE RELAYS

2.1 THE NATURE OF RELAY

Protective relays have been called sentinels and electric brains. From the economic point of view, relays are a kin to insurance; they protect the power utility from financial loss due to damage of equipment. From the underwriters' point of view they prevent accidents to personnel and minimize damage of equipment. From the customer's point of view good service depends more upon adequate relaying than upon any other equipment. The cost of this protection ranges between 1 and 2 per cent of the total cost of the power system.

In the dictionary, four definitions of relays will be found which deal with food races, post coaches, etc. but none even remotely fits this application. A protective relay is a responsive device to abnormal conditions on an electrical power system to control a circuit breaker, so as to isolate the faulty section of the system with the minimum interruption to service. To do this, relays must be able to decide promptly which circuit breakers are to trip in order to isolate only the faulted section(s). These relays must be designed, therefore, to be responsive to electrical quantities during normal and abnormal conditions. The basic electrical

quantities which may change in the transition from healthy to faulty conditions are current, voltage, direction, power factor (phase angle) and frequency |2,3,5|.

2.2 CLASSIFICATION OF RELAYS

Relays can be classified into five functional categories |3,10|:

a) Protective Relays, which detect defective lines, defective apparatus, or other dangerous or intolerable conditions. These relays can either initiate or permit switching or simply provide an alarm.

b) Monitoring Relays, which verify conditions on the power system or in the protection system. These relays include fault detectors, alarm units, channel-monitoring relays, synchronism verification, and network phasing. Power system conditions that do not involve opening circuit breakers during faults can be monitored by verification relays.

c) Programming Relays, which establish or detect electrical sequences. Programming relays are used for reclosing and synchronizing purposes.

d) Regulating Relays, which are activated when an operating parameter deviates from predetermined limits.

Regulating relays function through supplementary equipment to restore quantity to the prescribed limits.

e) Auxiliary Relays, which operate in response to the opening or closing of the operating circuit to supplement another relay or device. These include timers, contact-multiplier relays, sealing units, receiver relays, lock-out relays, closing relays, and trip relays.

In addition to these functional categories, relays may be classified by input, operating principle or structure, and performance characteristic:

a) Input:

- Current
- Voltage
- Power
- Pressure
- Frequency
- Temperature
- Flow
- Vibration.

b) Operating Principle or Structure:

- Percentage
- Multi-restraint

- Product
- Solid State
- Electromechanical
- Thermal
- Digital hardware relays.

c) Performance Characteristic:

- Distance
- Directional-overcurrent
- Inverse time
- Definite time
- Undervoltage
- Ground or phase
- High-or slow speed
- Phase comparison
- Directional comparison
- Segregated phase

2.3 DESIGN CRITERIA

A complex relaying system may result from poor system design or the economic need to use fewer circuit breakers. Considerable savings can be realized by using fewer circuit breakers and a more complex relay system. Such systems usually involve design

compromises requiring careful evaluation if acceptable protection is to be maintained.

The application logic of protective relays divides the power system into several zones, each requiring its own group of relays.

In all cases, the five design criteria listed below are common to any well-designed and efficient protective systems or system segment:

a) Reliability - the ability of the relay or relay system to perform correctly when needed (dependability) and to avoid unnecessary operation (security).

b) Speed - minimum fault time and equipment damage.

c) Selectivity - maximum service continuity with minimum system disconnection.

d) Economics - maximum protection at minimum cost.

e) Simplicity - minimum equipment and circuitry.

Since all these design criteria simultaneously, the necessary compromises must be evaluated on the basis of comparative risks |3,10|.

2.4 BASIC CONNECTION OF A PROTECTIVE RELAY

Fig. 2.1 shows schematically the basic connections of a relay to the trip coil of the circuit breaker which control the

power supply to the protected circuit when the relay contacts close, the high L/R ratio of the trip coil delays the build-up of current so that a fast breaker is tripped before the current reaches its steady value. For this reason, and because the duration of the trip coil current is only few cycles, the relay contacts need to have a continuous rating of only 5 amperes and yet operates a 30 ampere trip coil 50 times without any maintenance |2,5,6|.

After the breaker has tripped, its auxiliary switch, marked in Fig. 2.1, opens the highly inductive trip coil circuit and the relay can be reset when deenergised by the opening of the breaker. It is important however that the relay contacts do not chatter while the trip current is flowing, otherwise they will be badly burned. This is ensured either by non-bounce design or by the use of a magnetic hold-in coil on the relay or by a separate relay, known as a seal-in relay |2|.

2.5 PROTECTIVE RELAYS

Protective Relays can be classified into the following types:

(i) Time-over current Relays.

(ii) Reverse Power Relays.

(iii) Distance (Impedance) Relays.

(iv) Under voltage Relays.

(v) Differential Relays (Balanced Current Protection).

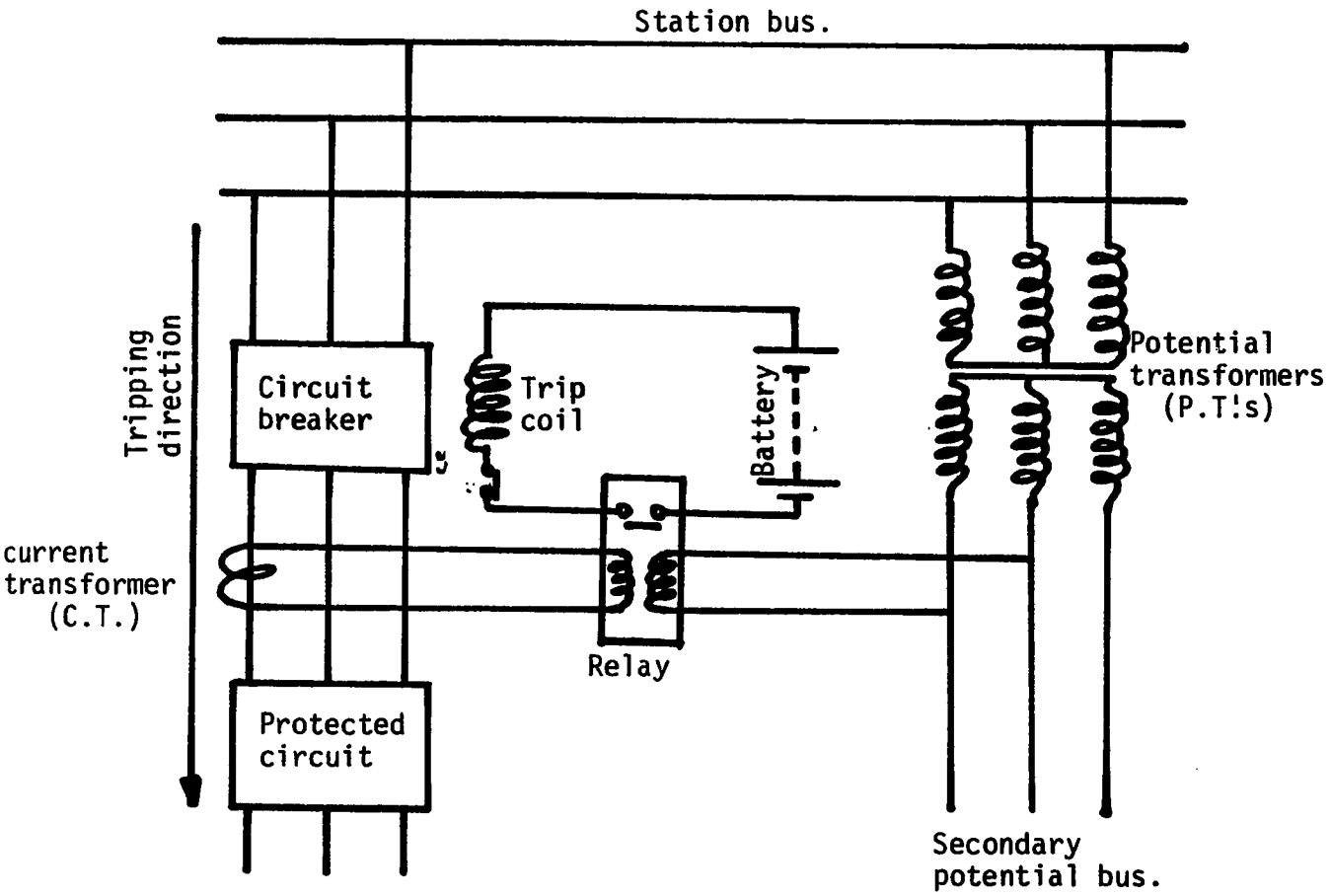


Figure 2.1. Basic connections of a protective relay.

2.5.1 Time-Overcurrent Relaying:

This scheme takes advantage of the fact that, when one section of the network develops a fault, current flows into it via the remaining healthy sections so that the faulty section has the most current.

If the overcurrent relays are provided with damping as shown in Fig. 2.2, their operating time will be inversely proportional to the current magnitude and the relay nearest the fault will operate fastest because it has the most current and hence will create the opening of its circuit-breaker and clear the fault before any of the more remote relays can do so.

2.5.1.1 Time-Current Characteristics:

Fault current can be used as a basis for selectivity only where there is an abrupt difference between its magnitude for a fault within the protected section and a fault outside it, and these magnitudes are almost constant. Where this is so, a current magnitude device can be used and selectivity can be obtained by grading current.

(a) Definite Time-Current Relays: An alternative to inverse time-current relays are the definite-time relays. Because their time is fixed, irrespective of current magnitude, such relays have to be graded in time. This is practical on radial lines or loops but the inverse relay is preferable for complex networks.

In radial or loop circuits, where there are several line sections in series, there is no difference in current between a fault at the

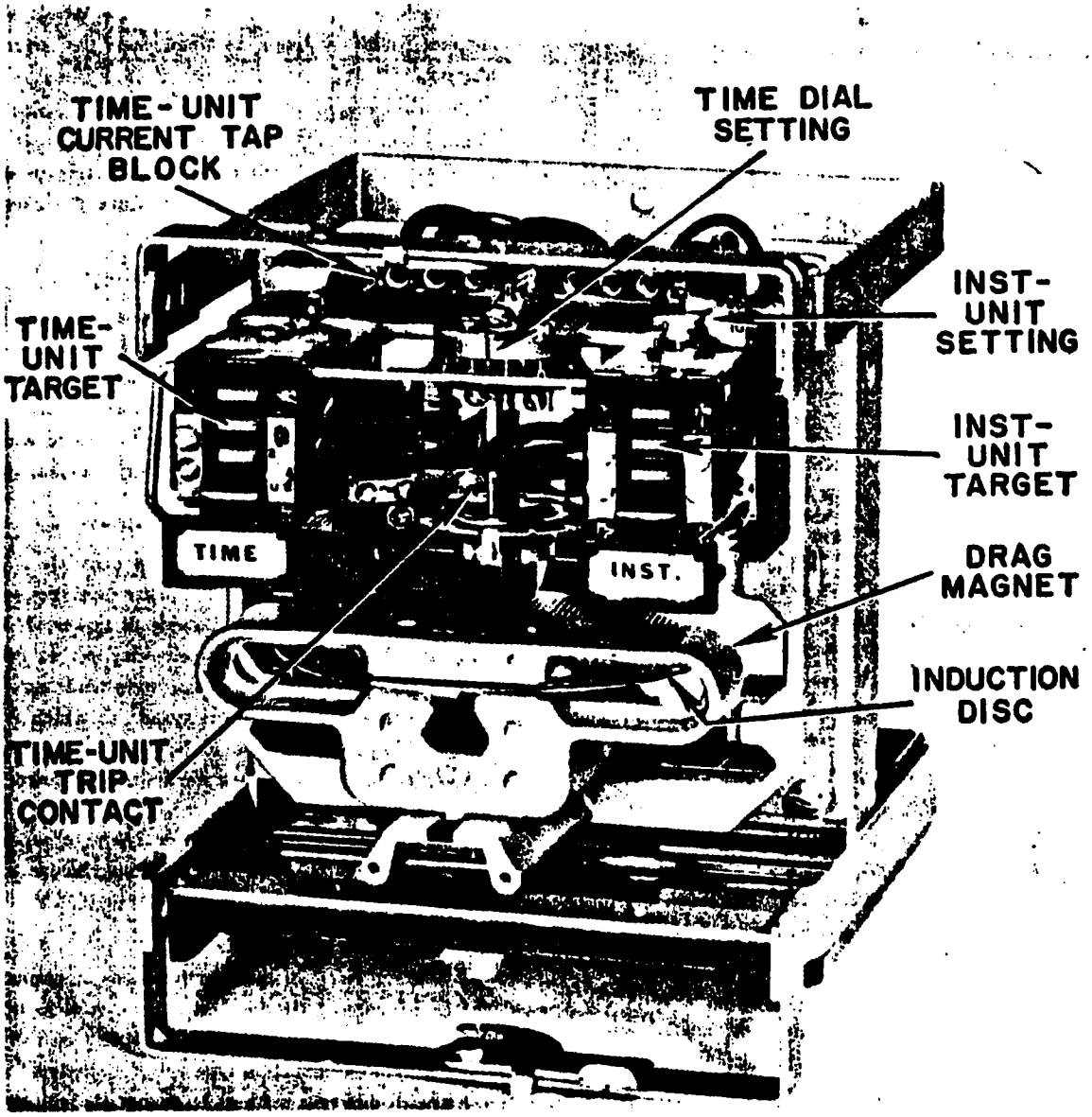


Figure 2.2. Typical Overcurrent Relay.

end of one section and a fault at the beginning of the next one. Consequently, it is necessary to add time discrimination with the time settings increased towards the source. Where there are many sections in series the tripping time for a fault near the power source may be dangerously high as shown in Fig. 2.3(a). This is obviously undesirable because such faults involve large currents and are very destructive if not removed quickly. The fundamental weakness of time-graded overcurrent relays is the fact that heaviest faults are cleared slowest |2|.

(b) Inverse Time-Current Relays: Where Z_s (the impedance between the relays and the power source e.m.f.) is small compared with that of the protected section Z_ℓ, there will be an appreciable difference between the current for a fault at the far end of the section ($I = \frac{E}{Z_s+Z_\ell}$) and the current for a fault at the nearer end ($I = \frac{E}{Z_s}$). In such a case a relay whose time is inversely proportional to the current ($It = K$) would trip faster for a fault at the end of the section nearer to the power source. Fig. 2.3 shows the resultant time-distance characteristics, compared with those of definite time relays. It will be seen that the inverse time relay can provide faster clearing times than the definite time relay, assuming the same selective intervals |2|.

The tripping time can be still further reduced by using a more inverse characteristic, such as $I^2t = K$.

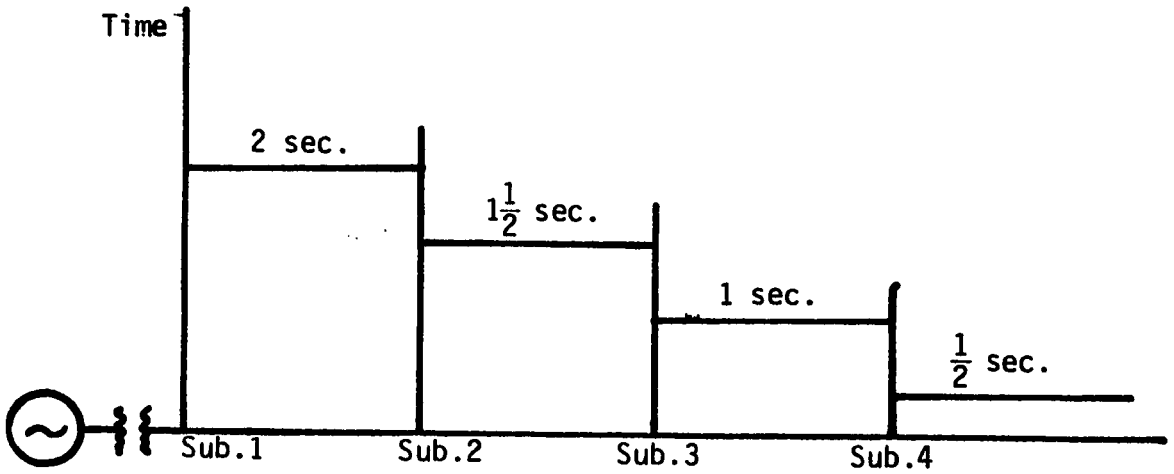


Figure 2.3(a). Definite time grading on radial circuit.

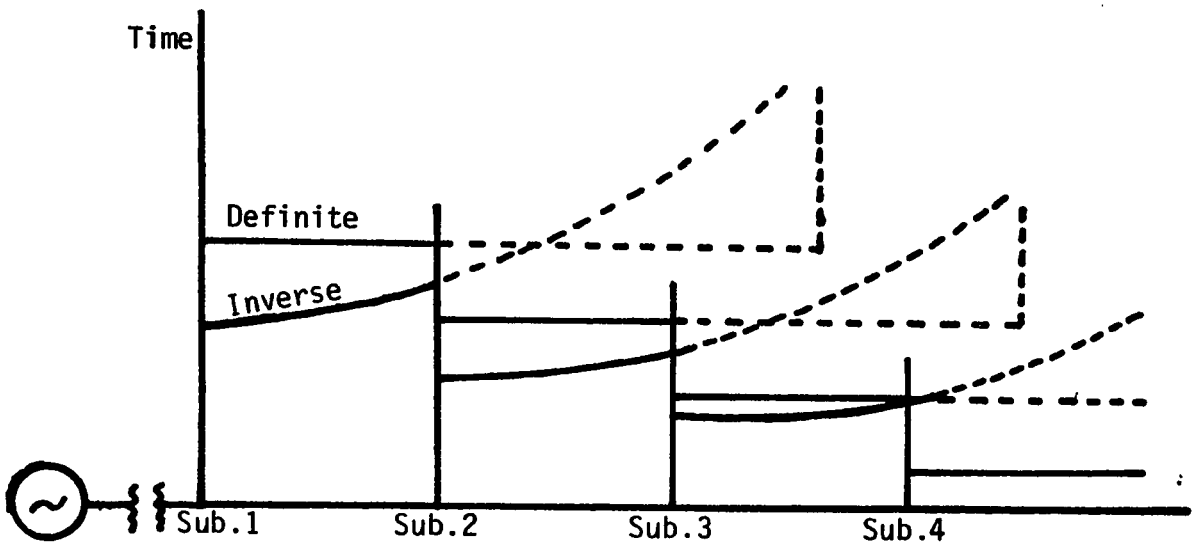


Figure 2.3(b). Definite versus inverse time current relaying.

(c) Extremely Inverse Time Overcurrent Relay ($I^2t=K$): For cases where the generation is practically constant and discrimination with low tripping times is difficult to obtain, because of the low impedance per line section, an extremely inverse relay can be very useful, one in which the time is inversely proportional to the square of the current, since only a small difference in current is necessary to obtain an adequate time difference |2|.

(d) Instantaneous Over-Current Relays: Another tool for reducing the tripping time for faults near the source is the high-set instantaneous relay which reduces the overall tripping times to a minimum because each relay, whether difinite or inverse, can be given the same time-multiplier setting, since it has only to be selective with the instantaneous relay in the next section as shown in Fig. 2.4 . In order that these instantaneous units shall be selective with each other, each one is set to pick up at a progressively higher value towards the source so that no relay can operate on the lower current value of a fault in the next section away from the source |2|.

2.5.2 Reverse Power Relays:

In certain equipment, such as generators, power will always flow outwards except if the generator has developed a fault or has lost its driving source, so that it is motoring and drawing power from the network. Such a condition is detected by a directional relay which closes its contacts for power (or a component of KVA

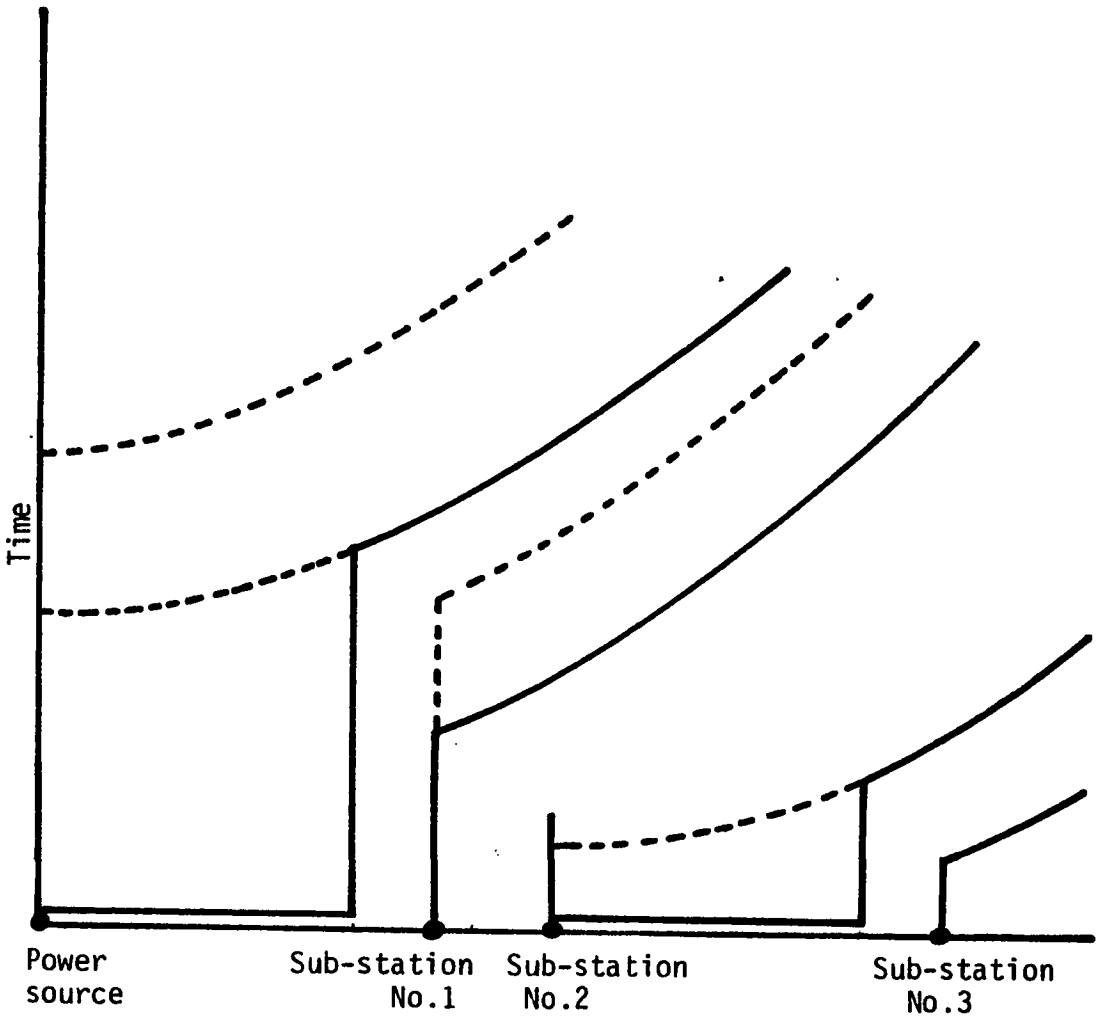


Figure 2.4. Reduction of time-settings by addition of high-set instantaneous overcurrent units.

at a suitable angle) flowing in an abnormal direction. Such relays work on the product of the circuit current and potential. If the product is positive, let us say, the torque closes the relay contacts; if negative, it holds them open. Thus the relay can be arranged to trip only when the current flows out from the bus. Consequently, by connecting a directional relay in series with each over-current relay, only the relays at the two ends of the faulty section will operate, thus isolating the fault without disturbing the other lines. Fig. 2.5 shows example of this relay |2|.

2.6 DISTANCE PROTECTION

Where time delay is undesirable distance relays are often used. For a line section of given impedance Z_L the current flowing through the section to a fault will produce a voltage $V = IZ_L$. Hence, if the relay compares V with I and is arranged to trip when $V < IZ$, it actually measures $Z = \frac{V}{I}$. Since Z is proportional to the length of the line the relay can be set to trip only for faults within the protected section of line |2-7, 10|.

So in a distance relay, instead of comparing the local line current with the current at the far end of the line, it compares the local current with the local voltage in the corresponding phase, or suitable component of them. Impedance, Reactance as well as admittance can be used for comparison in distance relaying. Fig.2.6 shows the simplest system consisting of feeders in series, such that power can flow only from left to right. If a short circuit occurs

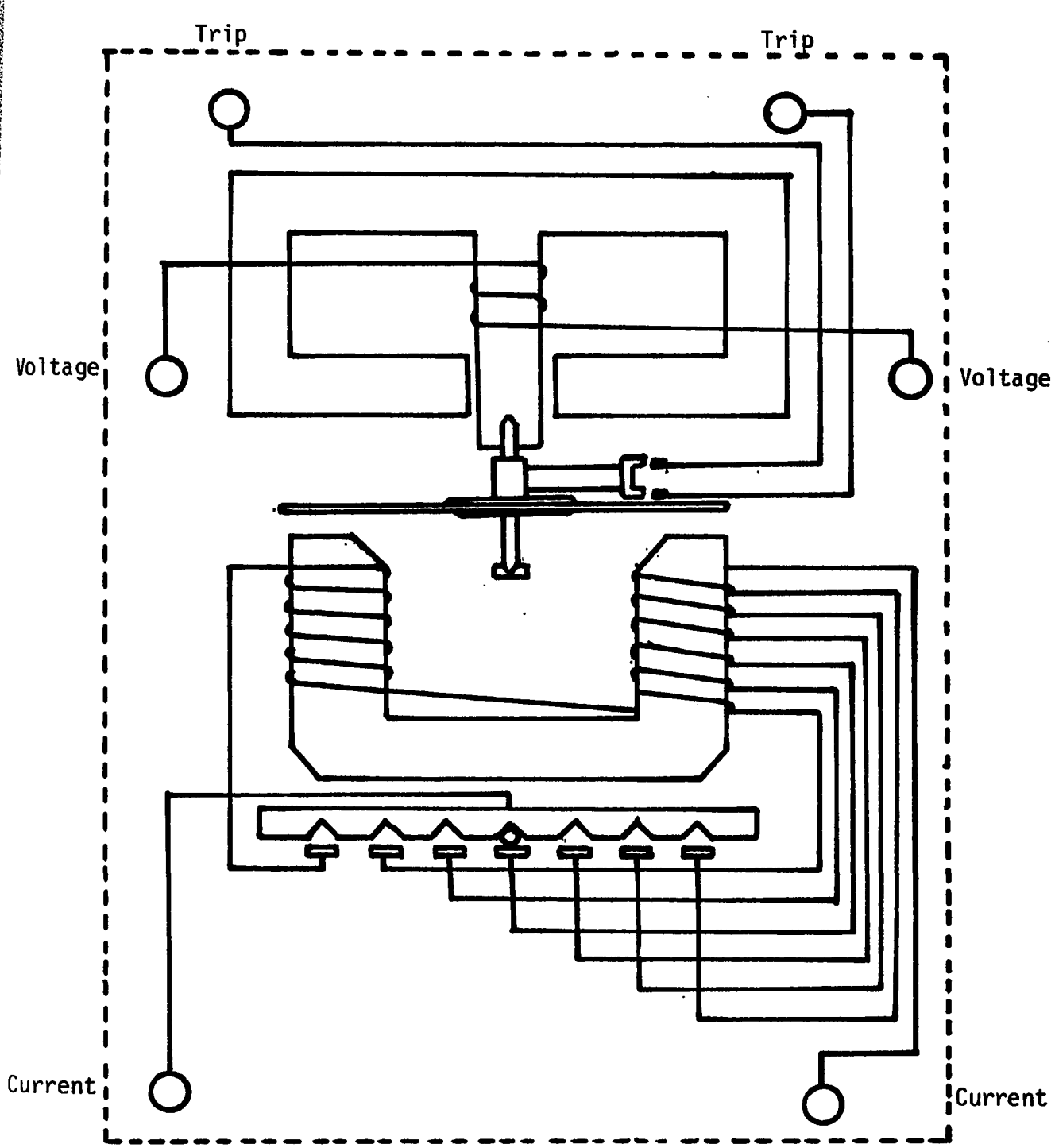


Figure 2.5. Reverse Power Relay.

at P between C and D, the impedances at A,B, and C are (Z_A+Z_B+Z), $(Z_B + Z)$, and (Z) respectively. The relays are set to operate with impedances less than Z_A, Z_B, and Z_C respectively, so that the only relay C will operate. Similarly, if the fault occurs between B and C, only relay B operates |27|.

2.7 BALANCED CURRENT PROTECTION

Parallel circuits of the same impedance should normally carry the equal currents. A fault in one circuit will increase the current in that circuit and operates a relay that compares the two currents. In the case of two parallel lines this is called 'current balance' or 'balanced current protection'. In the case of a generator with split windings it is called transverse differential current protection as shown in Fig. 2.7(a,b).

Buchholz relays will detect all faults that will occur under the oil, but it is possible to have a flashover above the oil at the bushings; although practically all such faults would involve ground, it is usual with large transformers to provide high-speed biased differential protection which detects such flashover and will also clear other heavy faults faster than Buchholz relays |2|.

A transformer differential relay compares the currents in the windings of the transformer through the medium of current transformers whose ratios are such as to make their secondary currents

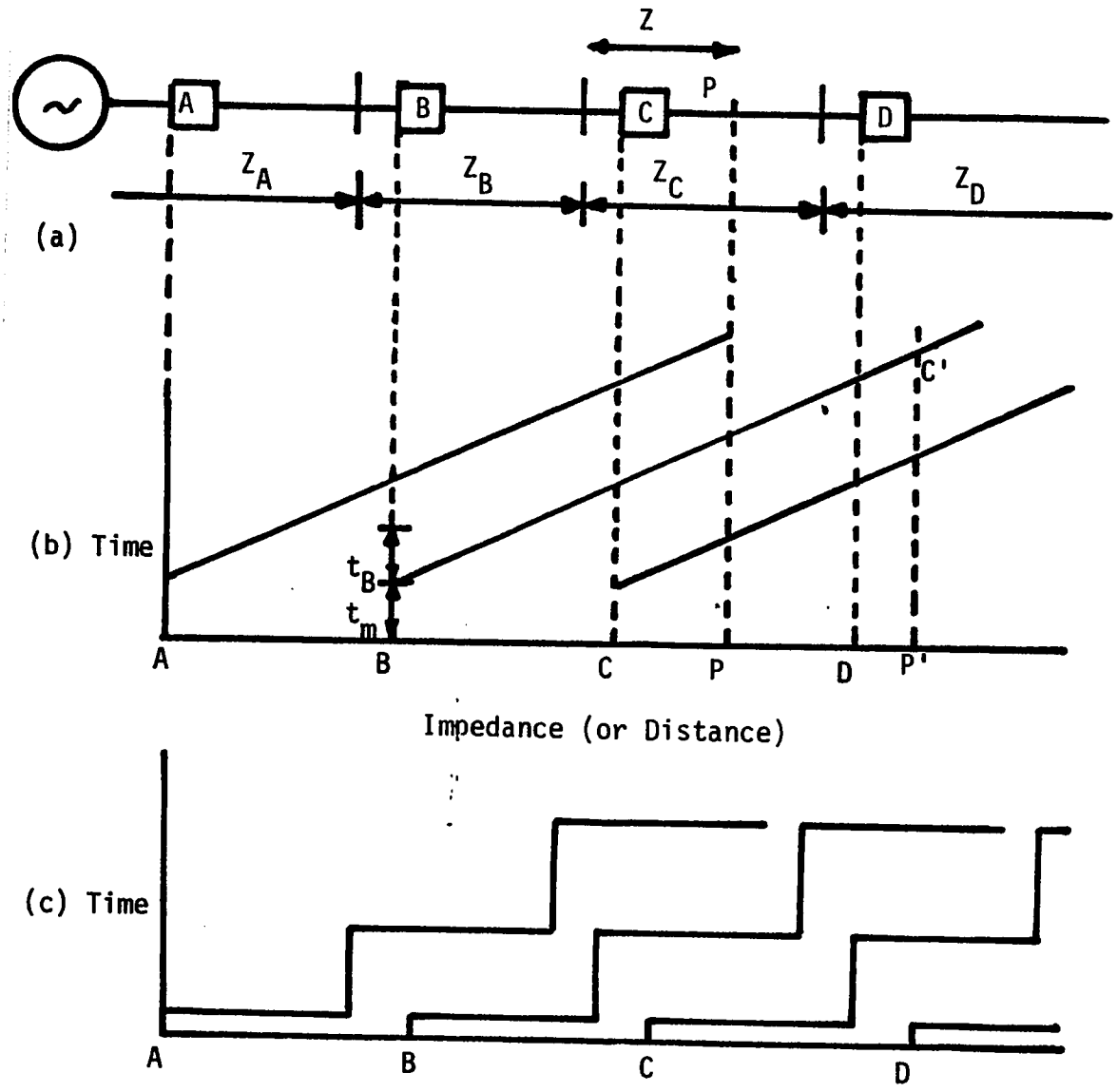
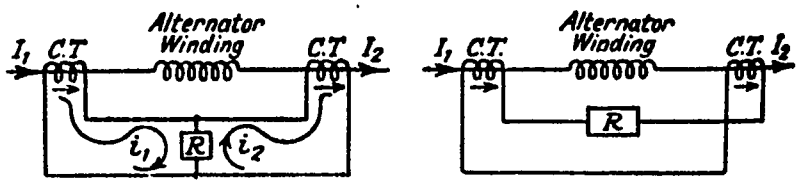
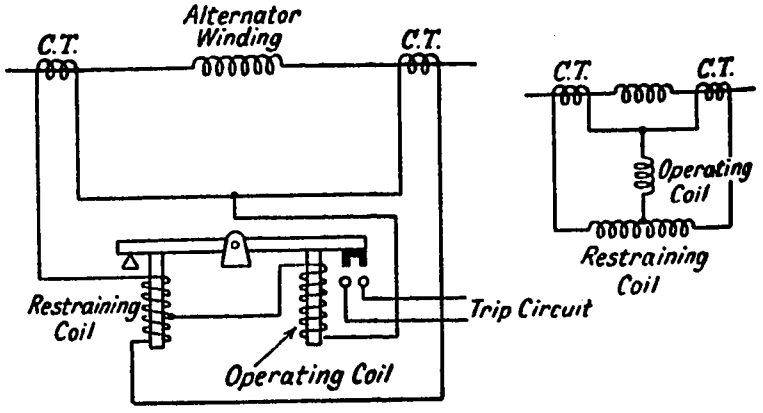


Figure 2.6. Distance or Impedance Protection.



Circuit Current

Opposed Voltage



Biased Beam Relay

Figure 2.7(a)

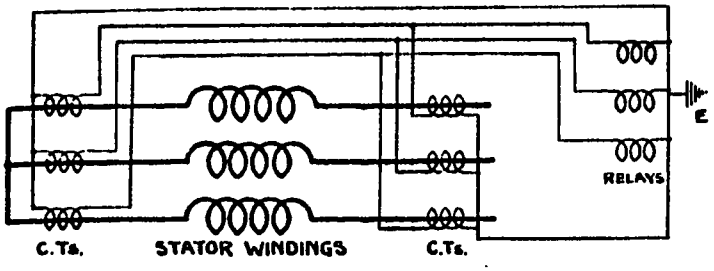


Figure 2.7(b). Merz-Price System for Alternator.

normally equal. Fig. 2.8 shows the relay in its simplest form; the polarity of the current transformers is chosen to make the current circulate normally without going through the relay, during load conditions and external faults, i.e. the relay coil receives the vector sum of the derived currents which is normally zero. Any fault within the transformers disturbs the balance and the relay operates.

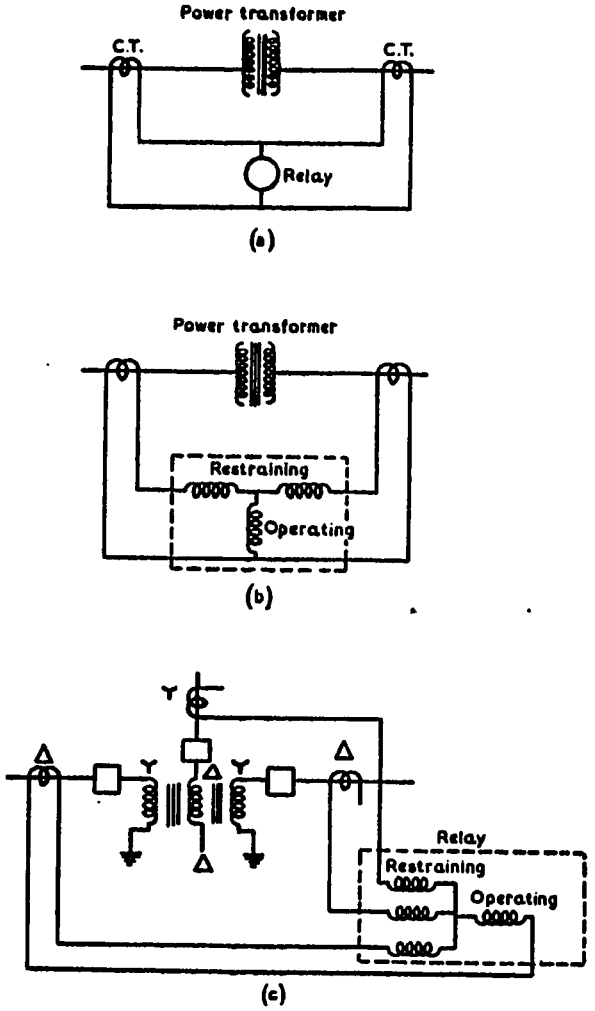


Figure 2.8. Differential protection of transformers
(a) Overall differential relay
(b) Percentage differential relay
(c) Three-winding transformer differential

3. HARDWARE DIGITAL OVERCURRENT RELAY

3.1 INTRODUCTION

As we have seen in the previous chapters, we had the electromechanical relays, the electronic relays, the solid state relays, and finally we had the protection using computers and minicomputers. Each one of these techniques has its own advantages and disadvantages which led to have an improved characteristics by making use of the advances in technology.

Hereby, the design and construction of a hardware digital overcurrent relay will provide virtually all the functions associated with the protection of power systems against over currents and faults. The new technology allows us to take a new look at some old problems and take advantage of improved performance characteristics.

These relays are based on sampling the current or voltage or both by an analog to digital converter, thus having a binary output equivalent to that analog input value. These binary outputs are then used with some logic circuit arrangements to achieve the same functions of the solid-state and the electromagnetic devices as will be explained.

3.2 CONTROLLER DESIGN PHILOSOPHY

Based on a study of the principles and features of existing electro-mechanical and solid-state protective relays, a list has been prepared of the desirable characteristics including those not available in existing relays, as well as the advanced concepts needed to accomplish these characteristics. The important factors and considerations that emerge from such a study are enumerated below.

(i) Reliability and provisions for updated digital back-up to permit bumpless transfer or bumpless switching.

(ii) Man-machine communication.

(iii) Economy of computation and comparison time.

(iv) Sampling errors and protection wind-up problems.

(v) Flexibility for adding more functions with system expansion and or expanded types of protection facilities.

(vi) Flexibility for adaption to most existing data facilities.

3.3 REQUIREMENTS OF DIGITAL RELAYS

The digital overcurrent relay is proposed to fulfill the

following requirements:

(i) The relay should come into action quickly on errors above certain settings for delay times in order to maintain the stability of the system.

(ii) The relay must permit parallel operation or mixed operation of several relays in the system or back-up protection with small offset. This necessitates that the relationship between current and operating time be accurately maintained.

(iii) The relay must differentiate between overload and overcurrents occuring in the system.

(iv) The deadband must be held to a minimum for better performance of the relay and should not be zero.

(v) The parameters governing the detection and control functions must be adjustable during operation; it must be possible to change them automatically to predetermined values when the state of the network varies.

(vi) Easy introduction of the reference inputs, introducing additional quantities into the control circuit.

(vii) The digital control circuit must not be affected by external disturbance.

(viii) It must be feasible to control all protective relays from a central point or central computer.

(ix) The main components must be subject to minimum wear or aging and must be reliable.

3.4 ADVANTAGES OF DIGITAL RELAYS

Recent advances in digital technology have managed to provide highly reliable digital devices at reduced cost. This leads to the feasibility of introducing digital techniques at the primary protection level, overcurrent, to solve some of the problems facing the power industry in fast response of protective devices |17,28|.

Some of the advantages that such relays have are:

(i) No inertia, friction, and mechanical wear problems. There are no moving parts, and no saturation in the cores.

(ii) Improved performance characteristics as a result of using the advanced techniques of electronics and integrated digital circuits.

(iii) High reliability, as the failure rate of microelectronic circuits vary between 0.004 and 3 failures per 10^6 hours while electromechanical parts vary between 0.1 and 50 failure per 10^6 hours |29|. They are smaller in size and lower in cost |9|.

(iv) Easier in maintenance since the whole circuit can be built in printed-circuit form and can be replaced or checked easily. Also paralleling two of these printed circuits and switching off between them during maintenance period will be easier.

(v) Easy interfacing with external controls such as on-line computer protection.

(vi) They are faster and impose considerably low burden on a.c. sources of current and voltage. Their lower burden characteristic may contribute to less expensive current and voltage transformers. This will increase the use of such relays for certain applications even if the greater speed may not be required for such application.

(vii) Flexible settings for the present stored preset values of currents in the registers and for the time setting of the delay units.

(viii) More applicable since one device can perform the job of several devices just by having certain adjustments and modifications as will be explained in modification circuits section.

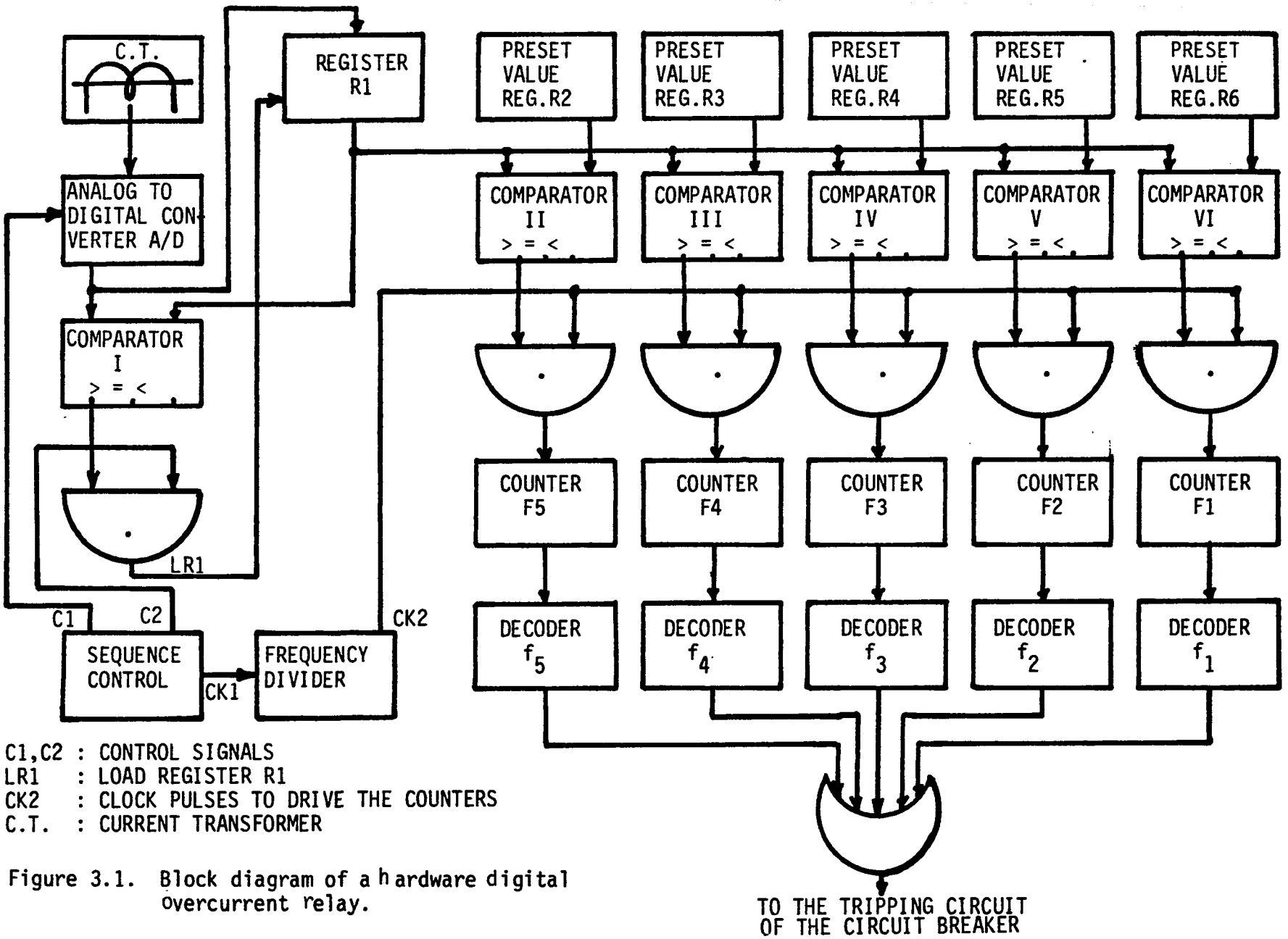
3.5 PRINCIPLE OF OPERATION

Operation of the digital overcurrent relay commences with the accumulation of an error signal. This process of error detection does not take place continuously, but is carried out in a systematic sequence during controlled time intervals. Due to the way in which the digital relay forms and acts upon an error signal, the steady state error of the governed quantity is always reduced to zero.

The hardware-based digital overcurrent relay is depicted in subsequent sections of this chapter.

3.6 DESIGN OF THE DIGITAL OVERCURRENT RELAY

The digital hardware overcurrent relay design consists of a number of basic building blocks dedicated by the control and protection requirements as illustrated in Fig. 3.1. The design for these functional blocks is generally fixed, but variable connections and couplings cater to particular situations required by the overall system.



C1,C2 : CONTROL SIGNALS
LR1 : LOAD REGISTER R1
CK2 : CLOCK PULSES TO DRIVE THE COUNTERS
C.T. : CURRENT TRANSFORMER

Figure 3.1. Block diagram of a hardware digital overcurrent relay.

3.7 BASIC BUILDING BLOCK STRUCTURE

The physical realization of the digital overcurrent relay is in the form of a modular structure. In this way, the detailed operation can be visualized clearly and any modifications and additions to the system can be performed easily. The digital relay comprises the following function blocks:

(a) Sampling and Analog to digital (A/D) conversion block.

(b) Error Formulation block.

(c) Actuating controller block.

(d) Sequence controller block.

Each of these function blocks has been built separately using discrete logic components and put together to form the hardware digital overcurrent relay.

3.8 SAMPLING AND A/D CONVERSION

Sampling is a technique of controlling the time at which information will be transferred or converted. Both digital and

analog signals can be sampled. A digital signal is a function in which both time and amplitude are quantized. The term quantization describes the process of representing a continuous variables by a set of discrete values. A digital signal may always be represented by a sequence of numbers in which each number has a finite number of digits.

The standard form for numerical processing of a digital signal is the binary number system. This system makes use only of the values 0 and 1 to represent all possible numbers. The number of levels (m) can be represented by a number having (n) binary digits (bits) given by $m = 2^n$. Conversely, if m is the number of possible levels required, then the number of bits required is the smallest integer greater than or equal to $\log_2 m$.

The process by which a digital signal is achieved will be illustrated by a simplified system as shown in Fig. 3.2(a).

The signal is first passed through a continuous-time pre-sampling filter to ensure that the highest frequency is within the bounds for which the signal can be recovered. The signal shown in Fig. 3.2(a) is read at intervals of T seconds by a sampler. These samples must then be quantized to one of the standard levels. One approach is that a sample is assigned the nearest level. The

signal is illustrated in Fig. 3.2(b). The pulses representing the signal have been made very narrow to illustrate the fact that other signals may be inserted or multiplexed in the empty space. These pulses may then be represented as binary numbers as illustrated in Fig. 3.2(c).

The process by which an analog sample is quantized and converted to a binary number is called analog-to-digital (A/D) conversion. In general, the dynamic range of the signal must be compatible with that of the A/D converter employed, and the number of bits employed must be sufficient for the required accuracy |31-32|.

The signal can now be processed by the type of unit appropriate for the application intended. This unit may be a general purpose computer or a microcomputer, or it may be a special unit designed specifically for this purpose.

At the output of the processor, the digital signal can be converted to analog form again. In this step, the binary numbers are first successively converted back to continuous-time pulses. The "gaps" between the pulses are then filled in by the reconstruction filter. This filter may consist of a holding circuit, which is a special circuit designed to hold the value of a pulse between successive sample values. In addition to a holding circuit, a basic continuous-time filter may be employed to provide additional smoothing between points.

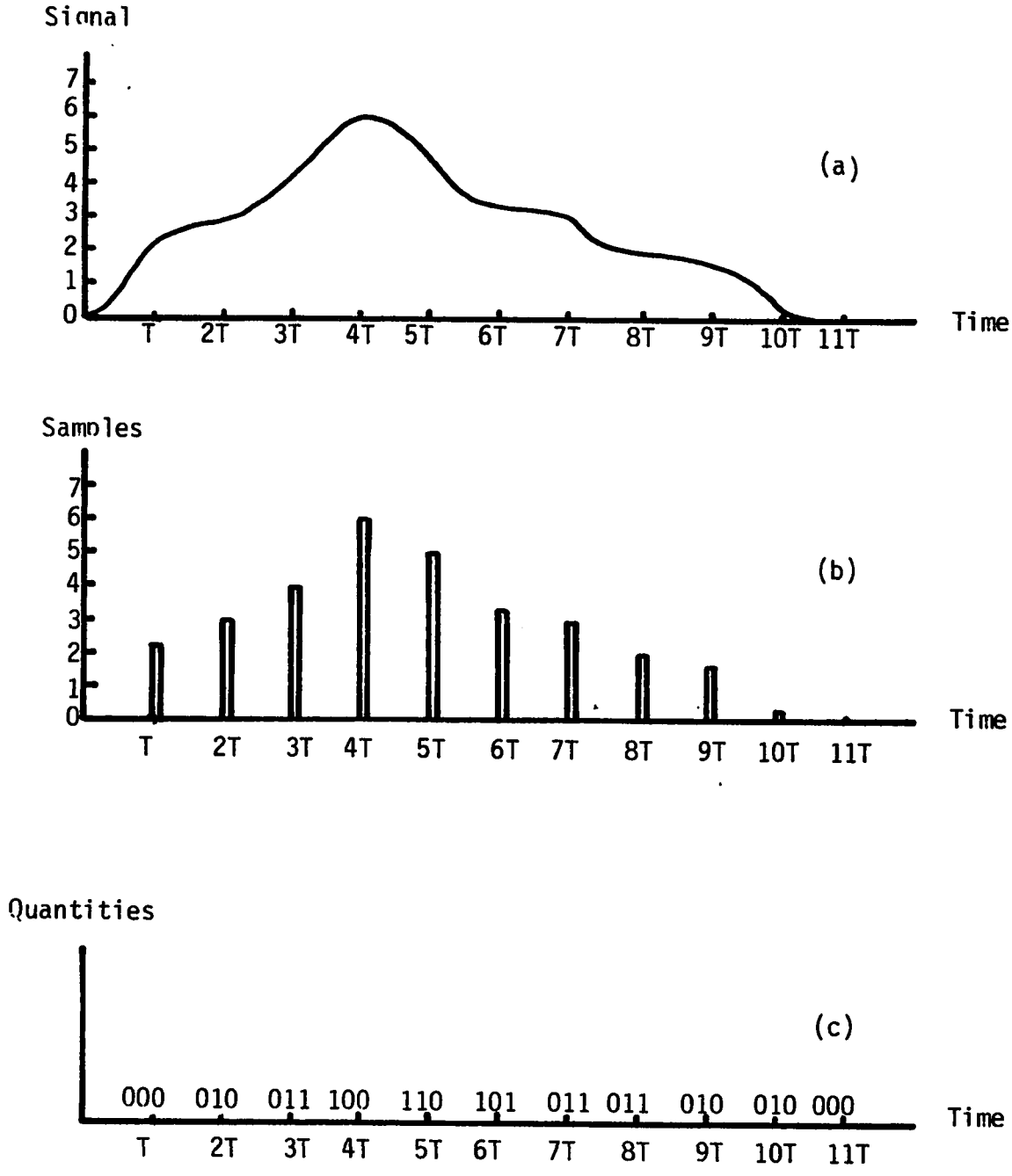


Figure 3.2. Sampling and digital conversion process.

An 8-bit analog to digital converter is shown in Fig. 3.3. It is necessary that $f_s \geq 2f_h$ where f_s is the sampling frequency and f_h is the highest possible frequency in the signal.

This relation between f_s and f_h is a statement of Shannon's Sampling Theorem, which states that a signal must be sampled at a rate at least as high as twice the highest frequency in the signal |30-32|.

3.8.1 Methods of Analysis:

Sampling of a function can be defined as taking a weighted mean of some physical quantity over a narrow range of some variable. This is also the definition of convolution |33|. Convolution in the time domain is analogous to multiplication in the frequency domain. Therefore, to determine the effects of sampling of a physical quantity over a limited range of the variable, the procedure is as follows:

1) Transform the function of the physical quantity into the frequency domain.

2) Transform the function of the sample variable into the frequency domain.

3) Multiply the transforms together to obtain the frequency spectrum of the sampled function and examine this spectrum.

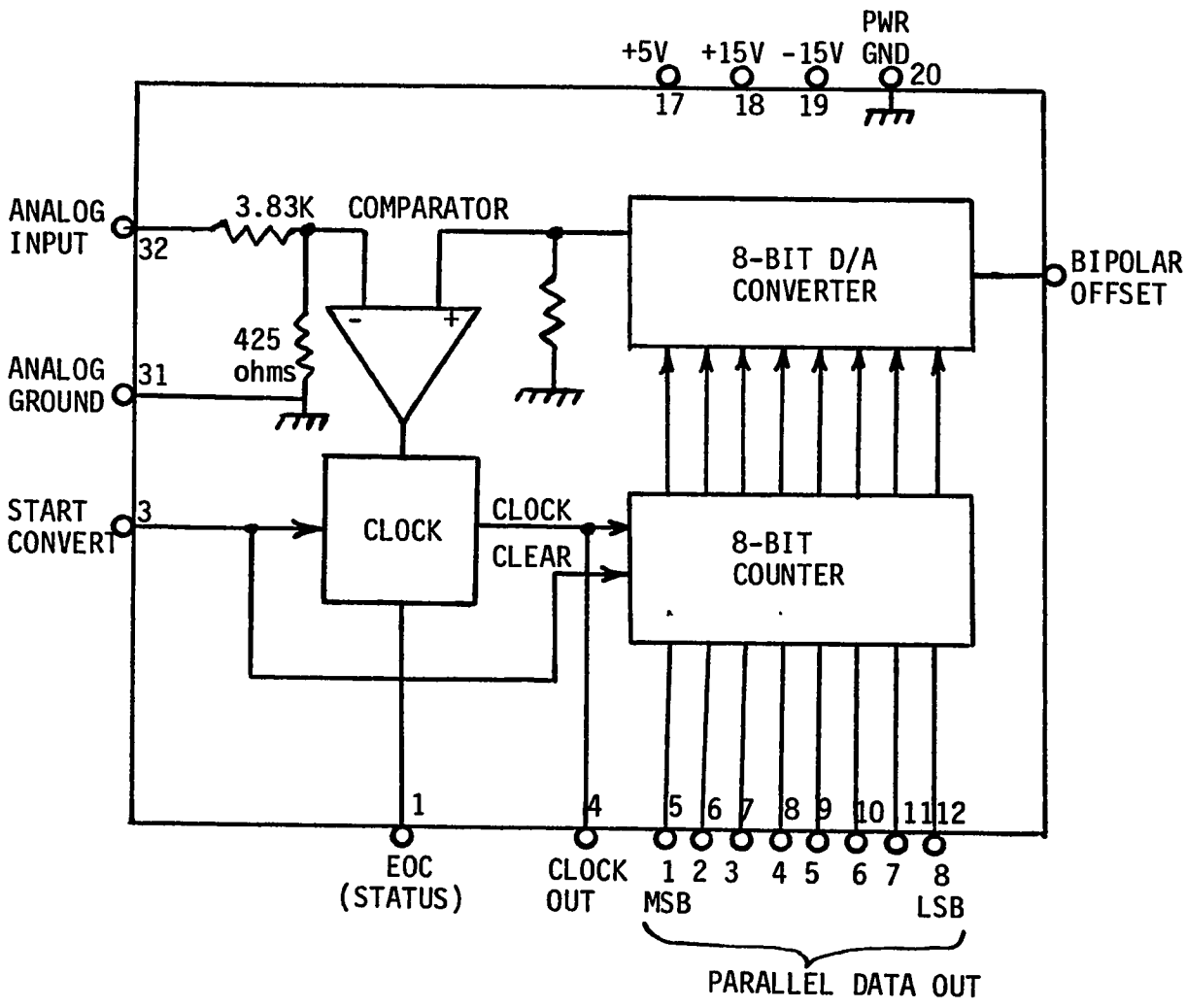


Figure 3.3. An 8-bit A/D converter.

3.8.2 Physical Quantity Transform:

During normal operation the voltage, $v(t)$, and current, $i(t)$, can be described by sinusoidal functions as follows:

$$v(t) = V_m \text{ Sin } 2\pi ft \qquad (3.1)$$

$$i(t) = I_m \text{ Sin } (2\pi ft - \phi) \qquad (3.2)$$

Where V_m is peak voltage.

I_m is peak current.

t is time

f is frequency in HZ.

and ϕ phase lag.

However on the occurance of a fault, a d.c. component and harmonics of current are likely. For a short duration after fault the current $i_F(t)$ can be approximated as follows:

$$i_F(t) = I_{dc} + I_m \text{ Sin}(2\pi ft - \phi) + I_3 \text{ Sin } (6\pi ft - \phi) \qquad (3.3)$$

Where I_{dc} is the dc component of the current

I_3 is the 3rd harmonic component of the current

Harmonic components of the current above the 3rd component are ignored.

Equation 3.3 can be considered to be a displaced real even function. Its transform is Hermitian so that the general form of the real and imaginary axis transforms are as shown in Fig. 3.4.

The function is scaled so that the length of period is 1. Therefore $\frac{1}{2}$ on the frequency scale is equivalent to 60 HZ. Since the magnitude of each frequency depends upon the exact system analysed, the components are chosen to be equal to one for illustrative purposes only.

3.8.3 Sample Functions:

Analysis is limited to sine and cosine functions which normally exist in power system.

For incorporation into a sample system for computer and digital relaying, the length of the function in the time domain must be limited. Since the 60 HZ current is to be used, the period from $-\tau$ to τ is $\frac{1}{60}$ seconds. The sample function to be transformed is given in Fig. 3.5.

The Fourier transform $F_c(s)$ of Cos π X is

$$F_c(s) = \int_{-\tau}^{\tau} \cos \pi X \, e^{-j2\pi sX} \, dX \qquad (3.4)$$

Since cos πX is an even function then,

$$F_c(s) = \int_{-\tau}^{\tau} \cos \pi X \cos 2\pi Xs \, dX \qquad (3.5)$$

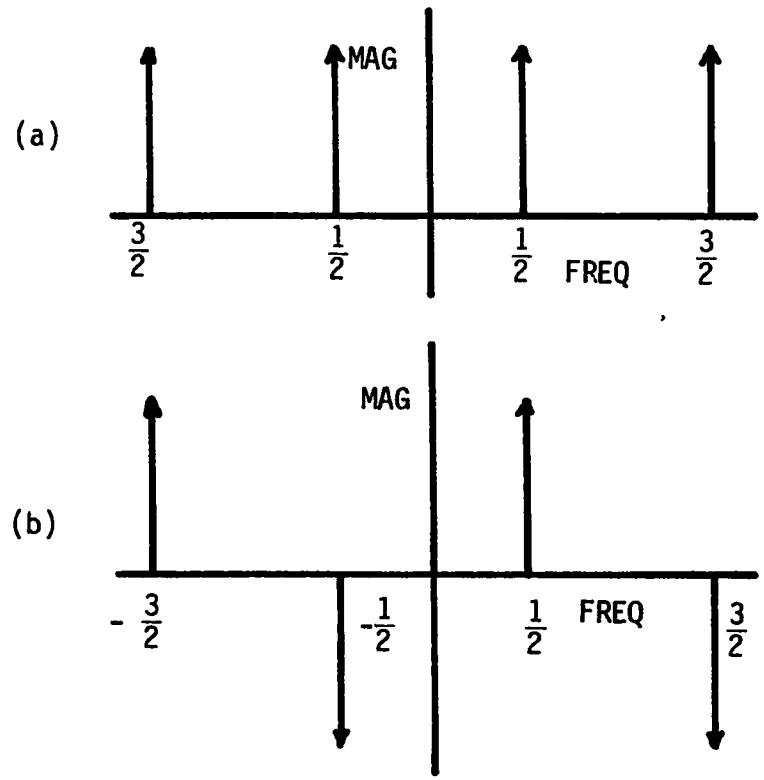


Figure 3.4. Fault Current Transforms a) Real Axis b) Imaginary Axis.

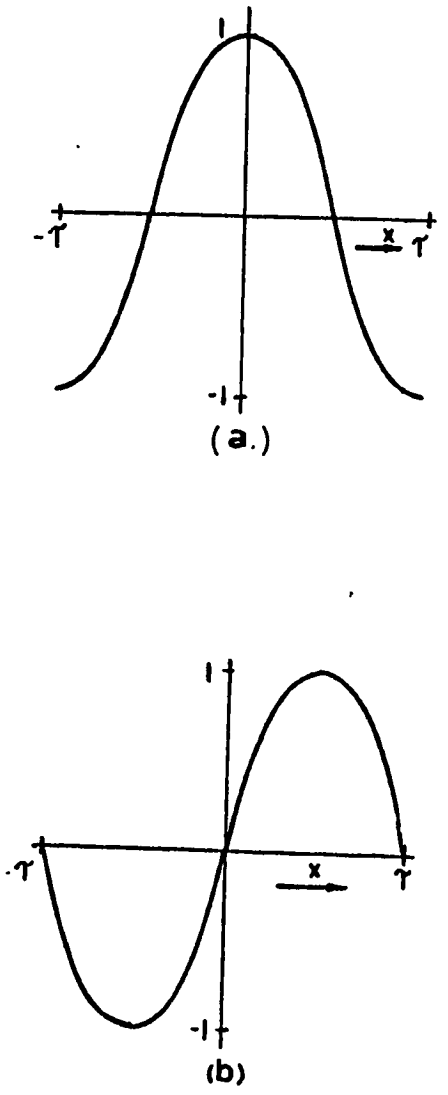


Figure 3.5. Time Domain Orthogonal Functions a) cos πx b) sin πx.

From trigonometric identities Eqn. (3.5) becomes,

$$F_C(s) = \int_{-\tau}^{\tau} \frac{1}{2} \cos 2\pi X \left(s + \frac{1}{2}\right) dX + \int_{-\tau}^{\tau} \frac{1}{2} \cos 2\pi X \left(s - \frac{1}{2}\right) dX \quad (3.6)$$

Solving

$$F_C(s) = \tau \frac{\sin 2\pi\tau\left(s + \frac{1}{2}\right)}{2\pi\tau \left(s + \frac{1}{2}\right)} + \tau \frac{\sin 2\pi\tau\left(s - \frac{1}{2}\right)}{2\pi\tau \left(s - \frac{1}{2}\right)} \quad (3.7)$$

From scaling we have

$$\tau = 1 \quad (3.8)$$

So that

$$F_C(s) = \frac{1}{2} \operatorname{sinc} 2\left(s + \frac{1}{2}\right) + \frac{1}{2} \operatorname{sinc} 2 \left(s - \frac{1}{2}\right) \quad (3.9)$$

Where we define $\operatorname{sinc} s = \frac{\sin \pi s}{\pi s}$ (3.10)

The Fourier transform $F_s(s)$ of $\sin \pi X$ is

$$F_s(s) = -\int_{-\tau}^{\tau} \sin \pi X \, e^{-j2\pi sX} \, dX \quad (3.11)$$

Since $\sin \pi X$ is an odd function then,

$$F_s(s) = \int_{-\tau}^{\tau} j \sin \pi X \sin 2\pi Xs \, dX \quad (3.12)$$

Solving

$$F_s(s) = \tau j \frac{\sin 2\pi\tau\left(s - \frac{1}{2}\right)}{2\pi\tau\left(s - \frac{1}{2}\right)} - \tau j \frac{\sin 2\pi\tau\left(s + \frac{1}{2}\right)}{2\pi\tau\left(s + \frac{1}{2}\right)} \quad (3.13)$$

Which is expressed as

$$F_s(s) = \frac{j}{2} \text{ sinc } 2(s - \frac{1}{2}) - \frac{j}{2} \text{ sinc } 2(s + \frac{1}{2}) \qquad (3.14)$$

Equations 3.9 and 3.14 describe the Fourier transforms of the X domain functions shown in Fig. 3.5. These transforms are illustrated in Fig. 3.6.

3.8.4 Sampled Function Frequency Spectrum:

With a change of variable from s to f multiplication of the components shown in Figs. 3.4(a) and 3.6(a) give the real axis frequency spectrum obtained by using the cosine function as a sample function |33|. Figures 3.4(b) and 3.6(b) give the resultant imaginary axis spectrum. Examinations show that cosine sine functions have a high rejection to dc and to high order harmonics. Limiting the length, however, flattens and shifts the frequency spectrum around the fundamental. For the cosine and sine waveforms the displacement in frequencies is slightly above and below 60 HZ respectively |33|.

3.8.5 Sampling Technique:

The A/D converter used operates on the counter method of conversion. It uses a digital counter to step the output of the D/A converter until it is equal to the amplitude of the input signal. At this time the conversion is completed and the parallel output data is valid.

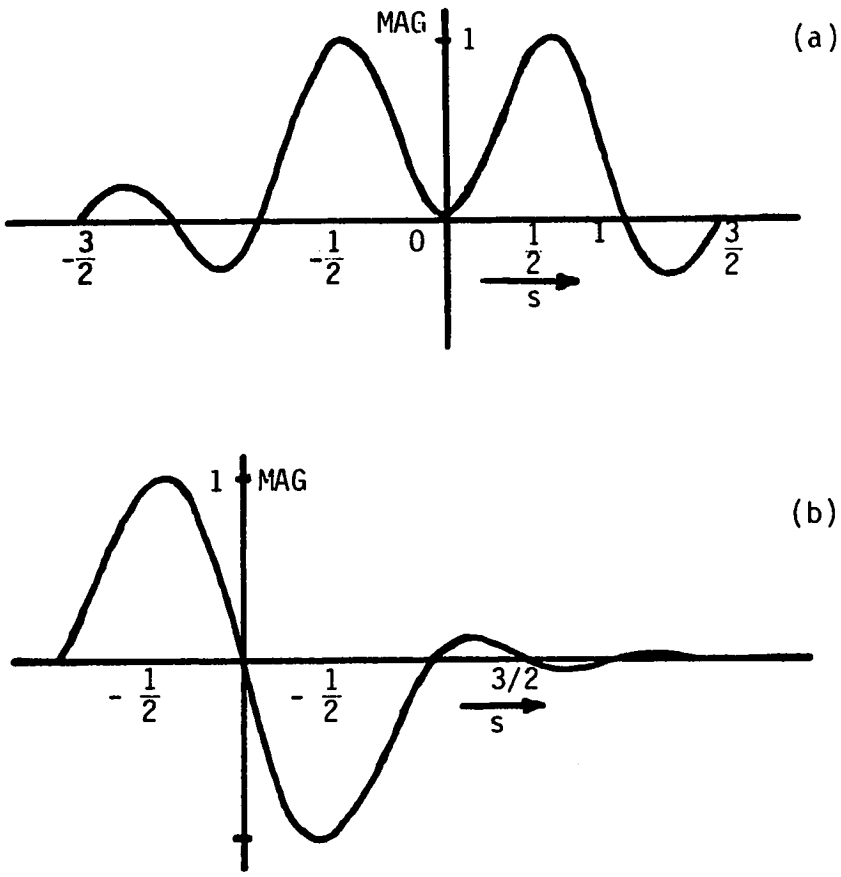


Figure 3.6. Fourier transforms of sine, cosine functions
a) $F_c(s)$ b) $F_s(s)$.

An 8-bit A/D converter was used to convert the analog input current to an output digital binary value. The input current signal has the power supply frequency of 60 HZ. The sampling rate was 1 KHZ, which is much higher than the signal frequency and quite applicable for the purpose of protection [33].

The detailed information and specifications of the A/D and D/A converters are given in Appendix A.

Test results on sampled current waveforms are given in chapter 4.

3.9 ERROR FORMULATION BLOCK

Once the input signal has been sampled and converted into a digital form, it can be used and processed for the determination of fault/no fault situations. This block consists of the following components as shown in Fig. 3.7.

(i) Digital Comparators I to VI.

(ii) Parallel-in-Parallel-out digital registers R1 to R6.

(iii) Two-input "AND" gates A1 to A6.

Digital comparators are needed to know whether a binary number A is greater than, equal to, or less than another number B. Four-bit comparators are available in the market. In our system, 8-bit comparators are needed. This can be obtained by cascading

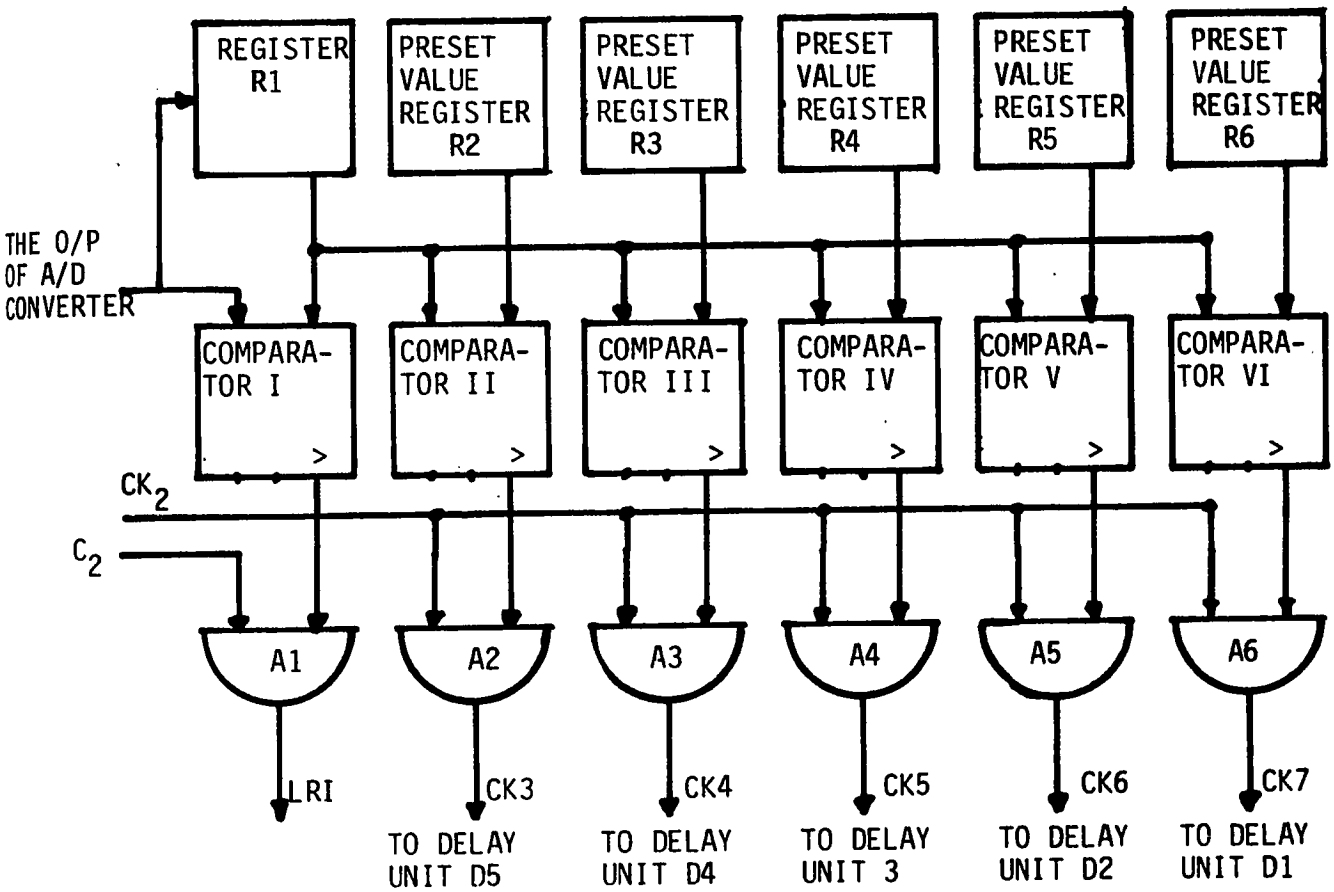


Figure 3.7. Error Formulation Diagram.

two 4-bit comparators. Figure 3.8 shows the 4-bit digital comparator used. The detailed information about comparators is given in Appendix B.

Digital registers are used to store the digital data. They consist of flip-flops. 8-bits parallel-in parallel-out registers are needed. Two 4-bit registers were used at the same time to get these 8-bit registers. The registers used, feature parallel and serial inputs, parallel outputs, made control, and two clock inputs. Parallel loading is accomplished by applying four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the output after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Figure 3.9 shows the circuit diagram of the register used.

Detailed information about the registers is given in Appendix C.

3.9.1 Error Formulation Process:

The A/D converter is connected to the secondary of the current transformer. At each sampling pulse, C1, a current sample is taken and is converted by the A/D converter to an equivalent binary value outputted of the A/D converter. At the beginning, the contents of Register R1 are reset to zero. Then the binary value of the sample is compared with the contents of register R1. The comparison is done using comparator I. If the binary value of the

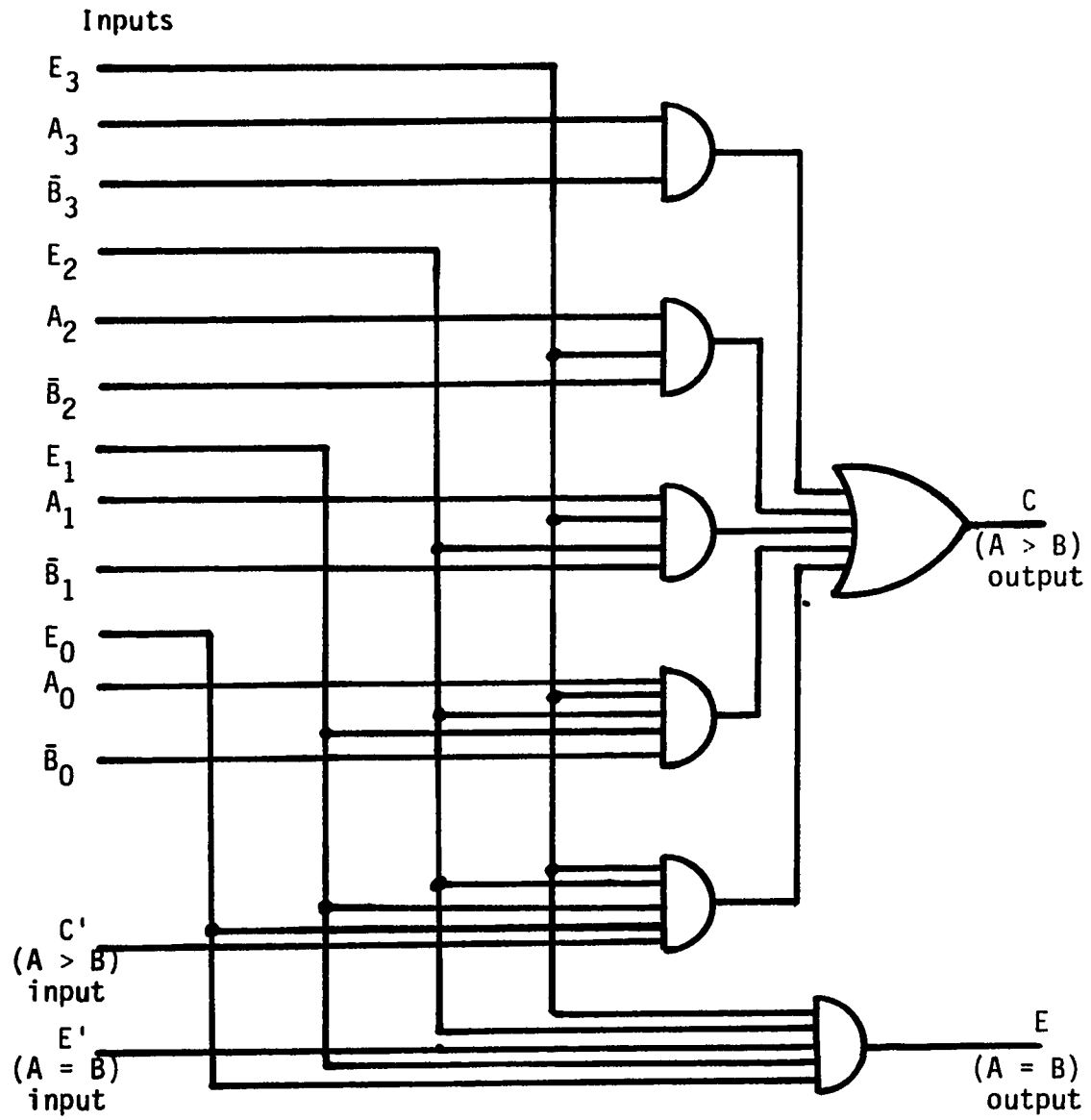


Figure 3.8. A 4-bit magnitude comparator.

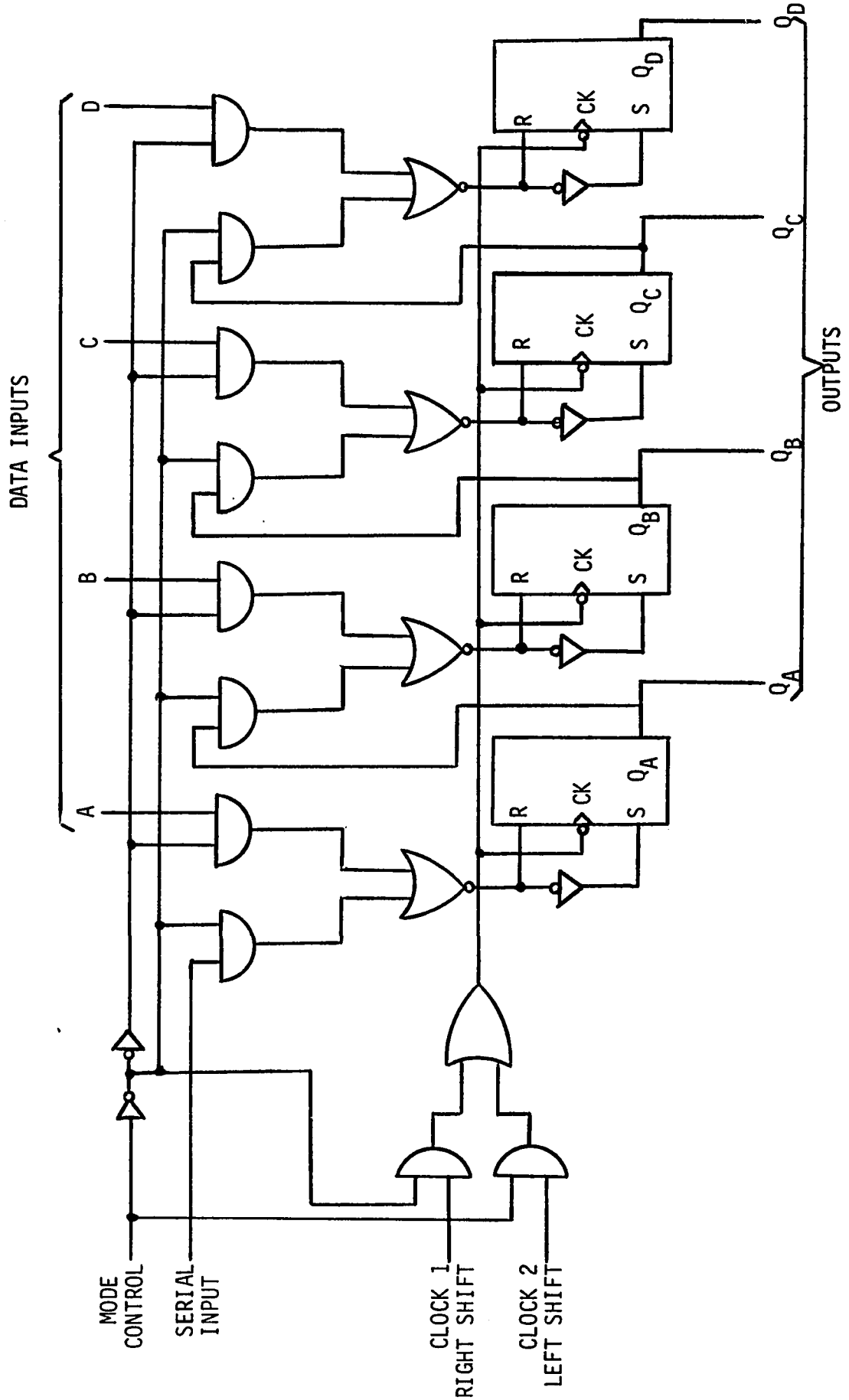


Figure 3.9. 4-bit parallel Access Shift register.

sample is larger than the contents of register R1, it will be transferred to register R1 to replace the previous smaller value. This transfering action takes place after a time period controlled by the control signal C2. As a result of C2, the loading signal LR1 will trigger the register R1 to store these new data. On the other hand if the binary value of the sample is less than or equal to the value already exist in R1, then no transfer of data will occur, and we have to wait for the next sample. This process is repeated 1000 times per second. It should be noticed here that the register R1 will always contain the largest value (the peak value of the input signal).

The contents of register R1 will be continuously (each 1 m.sec.) compared with the preset values of currents stored in registers R2 to R6 using comparators II to VI respectively. The preset values in the registers R2 to R6 are set to different values of the full load current multiples.

These preset values are used as controllers for the operating performance of the relay.

For our laboratory model relay, these registers contain the following values:

Register R2 contains a multiple of 1.25 times the full load current to work for overload section of the characteristic.

Register R3 contains a multiple of 5 times the full load current for low values of short circuit currents.

Register R4 contains a multiple of 10 times the full load current for moderate values of short circuit currents.

Register R5 contains a multiple of 20 times the full load current for extreme short circuit currents.

Register R6 contains a multiple of 40 times the full load current for the most dangerous undamped short-circuit currents existing in pure reactive circuits or resonating circuits.

If the contents of register R1 are greater than the contents of any or all of the registers R2 to R6, an output of the corresponding comparator will give a high level at the output assigned "A>B" which will be ANDed with the clock pulses CK_2 to set the respective counter.

3.10 ACTUATING CONTROLLER BLOCK

This block consists of the following components as shown in Fig. 3.10.

(i) Counters: F1 to F5.

(ii) Decoders: f1 to f5.

(iii) 5-input OR gate.

The delay unit, D, consists of one counter and one decoder as follows:

The Delay unit D_1 consists of the counter F_1 and the

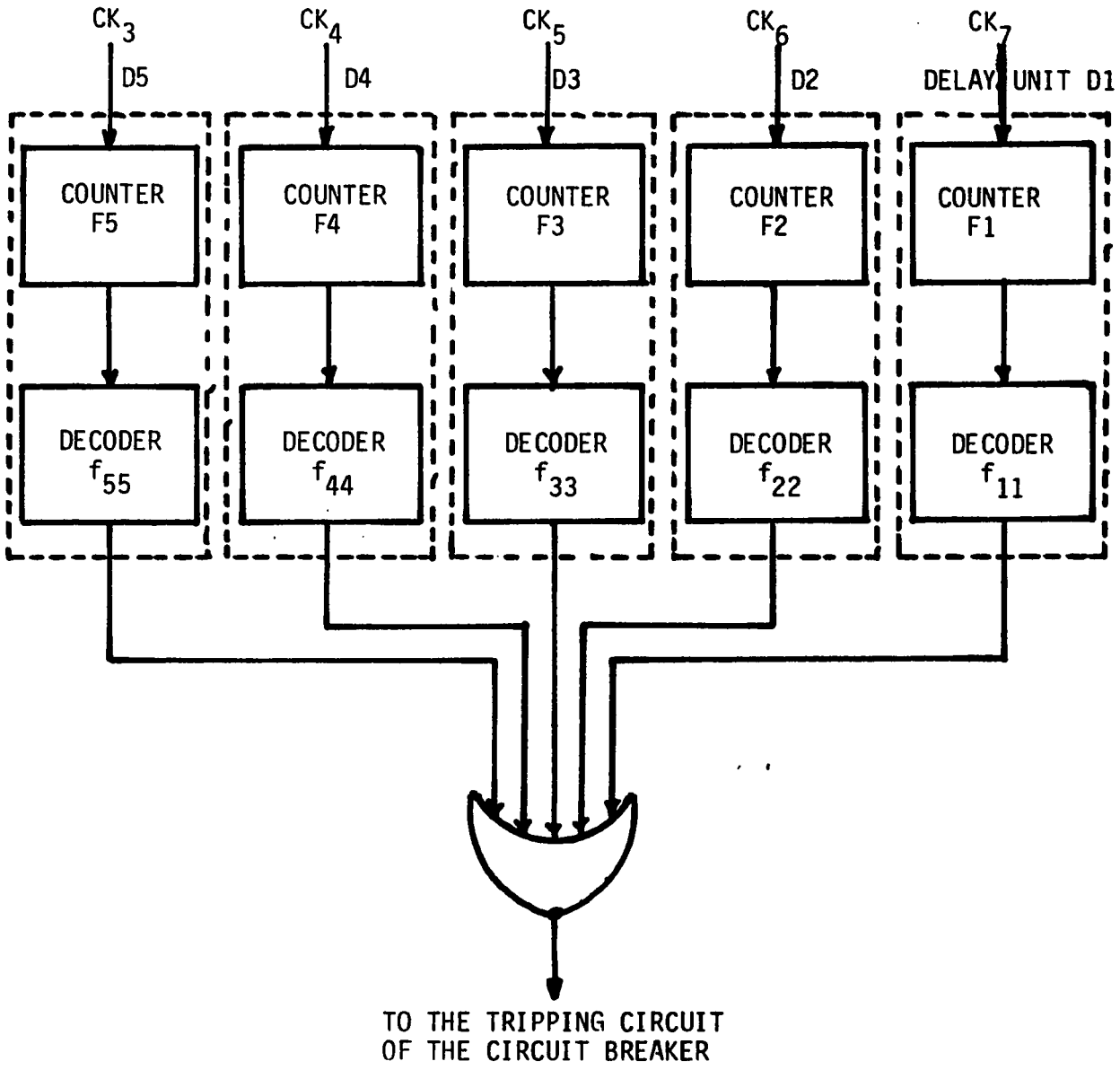


Figure 3.10. Actuating Controller Block.

decoder f1.

The Delay unit D2 consists of the counter F2 and the decoder f2.

The Delay unit D3 consists of the counter F3 and the decoder f3.

The Delay unit D4 consists of the counter F4 and the decoder f4.

The Delay unit D5 consists of the counter F5 and the decoder f5.

The delay counters are 12-bit counters, to have $2^{10} = 4096$ combinations. This makes it easy to use the relay in a very wide range of applications. The 12-bit counters are obtained by cascading three 4-bit counters. A 4-bit counter circuit diagram is shown in Fig. 3.11. To use the maximum count length of these counters, the B input is connected to the Q_A output. The input count pulses are applied to the input A and the outputs are as described in the Function Table I and the Reset/Count Function is in Table II.

The logic functions of the decoders are chosen to give the required time delays as given in Table III. Using different counting frequencies (CK2), the delay times associated with each logic function can be varied and thus new shifted characteristics for several applications could easily be created. This can be illustrated as shown in Table IV.

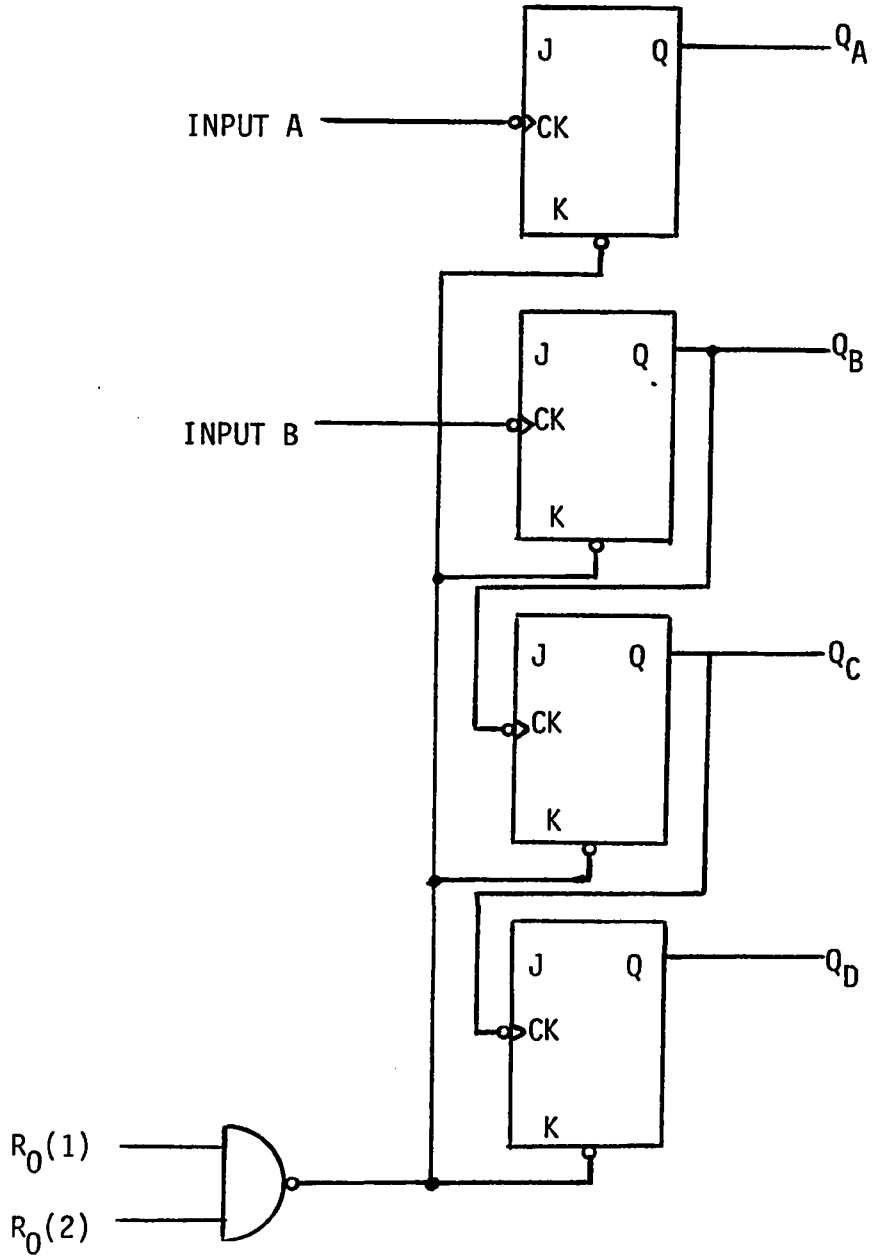


Figure 3.11. 4-bit binary counter.

TABLE I. Count Sequence.

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

TABLE II. Reset/Count Function.

RESET INPUT		OUTPUT			
$R_0(1)$	$R_0(2)$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	—	COUNT		
X	L		COUNT		

TABLE III. Logic Functions of Decoder.

Logic function	Binary Code	Weight of Delay
$f_{11} = \bar{L}\bar{K}\bar{J}\bar{I}$ HGFE DCBA	0000 1111 1111	255
$f_{22} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}$FE $\bar{D}\bar{C}$BA	0000 0011 0011	51
$f_{33} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}$E $\bar{D}$C$\bar{B}\bar{A}$	0000 0001 0100	20
$f_{44} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}\bar{E}$ D$\bar{C}\bar{B}\bar{A}$	0000 0000 1000	8
$f_{55} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}$C$\bar{B}$A	0000 0000 0101	5

TABLE IV. Different Counting Frequencies and the Corresponding Time Delays.

Counting frequency CK2	Time Setting	Associated time delays with f_{55}(ms)	f_{44}(ms)	f_{33}(ms)	f_{22}(ms)	f_{11}(ms)
500 Hz	1	10	16	40	102	510
250 Hz	2	20	32	80	204	1020
125 Hz	3	40	64	160	408	2040
62.5 Hz	4	80	128	320	816	4080

The logic diagrams of these decoders are shown in Fig. 3.12.

It should be known that once we got the high level at one or more of the "A > B" output of the comparators, a fault is detected and the relative counter should be set by one of the relative clock pulses CK3 to CK7 respectively, which are used to set the counters of the delay units D1 to D5. The outputs of these counters are strapped to give the required delay times. These delay times are chosen in a way to suit the different types of applications. These strappings are performed by the decoders f1 to f5. The logic functions of these decoders are given also by f11 to f55.

Thus by choosing the contents of the registers R2 to R6 and the corresponding delay times, one can achieve the different time current characteristics required for any application.

When any one of the logic functions f11 to f55 is verified, which means that the relative counter has been set to required value, a tripping signal goes through the OR gate to open the appropriate circuit breaker.

3.11 SEQUENCE CONTROLLER

The sequence controller circuit, used to control the sequence of operations of this relay, uses the multiphase-clock principle as shown in Fig. 3.13.

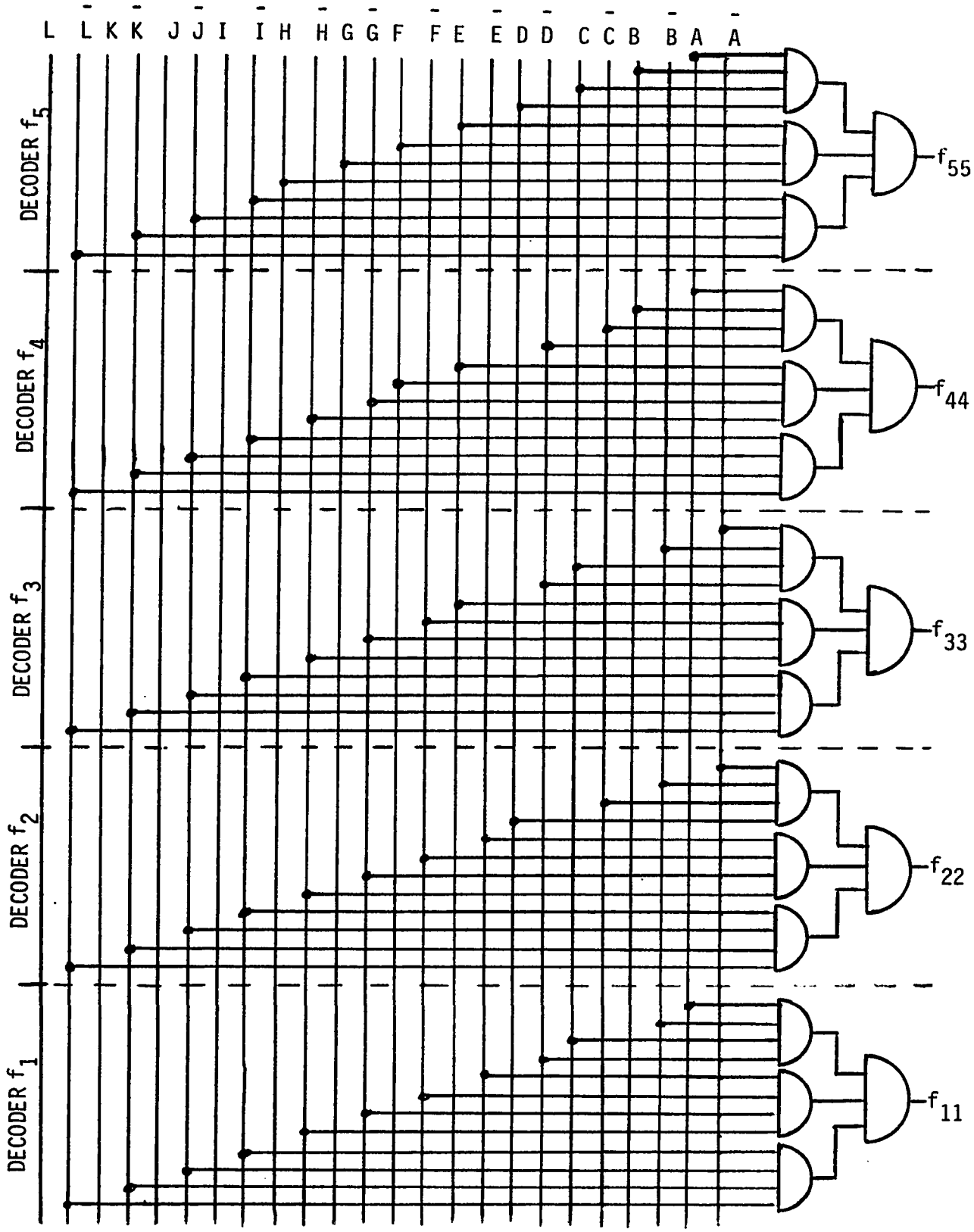


Figure 3.12. Logic Diagram for the Decoders.

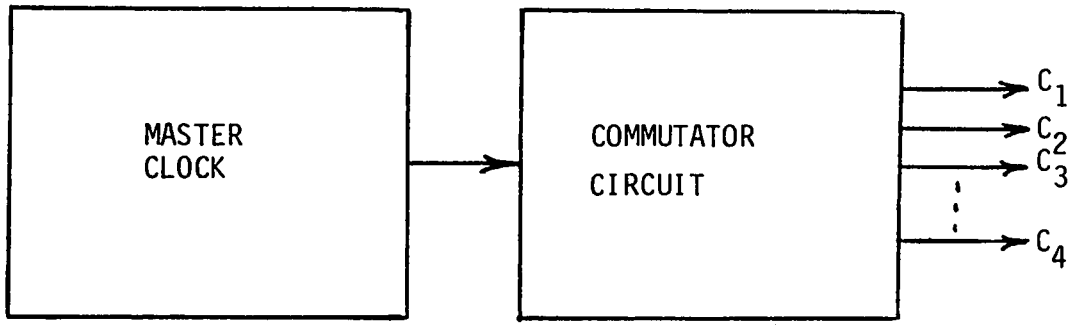


Figure 3.13. Sequence Controller Circuit.

The commutator circuit may consist of a ring counter or a binary counter with decoder. This decoder will successively gate clock pulses one at a time, on a set of lines. The code of certain operation will be chosen according to the time sequence of the operation steps and the length each step needs to be completed |34|.

The operation of the digital overcurrent relay needs only two control signals, in particular, C1 and C2. C1 is used as the start convert signal to the A/D converter and C2 is used to order the transfer of data from the output of the A/D converter to the register R1 after giving sufficient time for the conversion process to finish.

A 4-bit binary counter is used for the commutator circuit. A 2-bit binary counter is adequate to give four codes or four control signals. The reason for using the 4-bit binary counter is to expand the codes to be 16,which will allow for further extensions and different applications of the circuit for distance relays, impedance relays, power relays, etc.

As mentioned earlier, a sampling frequency of 1 KHZ is used. A 4-bit counter can give as many as 16 output combinations. The counter will reach its full scale after 16 input pulses. The first output combination (0000) will be used as the start convert control signal. Thus every time the counter reaches 0000 output, a new sample will be taken. To maintain our sampling rate to 1 KHZ, the counter should pass 0000 output every 1 m.sec., i.e., the master clock should give a pulse every $\frac{1}{16}$ m.sec. which corresponds to a master

clock frequency of 16 KHZ. The output combination 0101 will be used as the control signal C2. The state diagram of the controller is as shown in Fig. 3.14.

The sixteen different output combinations of the commutator circuit counter for a counting frequency of 16 KHZ are shown in Table V.

The control signal C2 is chosen as 312.5 μ sec. after the start convert signal, because the conversion process takes 200 μ sec. to be completed. The logic diagram which gives these control signals C1 and C2 and their photocopy are shown in Fig. 3.15. Note the delay of C2 behind C1. It is noticed that the control signal C1 occurs every 1 m sec. (a frequency of 1 KHZ), which means that the master clock frequency (16 KHZ) has been divided by 16. Thus the counter has served as a frequency divider. The same principle will be used to get the counting frequencies which will drive the delay counters. This will help to minimize the number of separate clocks.

The 1 KHZ which is already obtained as a result of dividing 16 KHZ by 16 will be divided further more by 2,4,8 and 16 to get different delay times for the same logic functions f11 to f55.

In this application, the 16 KHZ was divided by 16 to get 1 KHZ frequency as the start convert signal. This 1 KHZ was divided by 4 to get a counting frequency of 250 HZ (T=4 m.sec.).

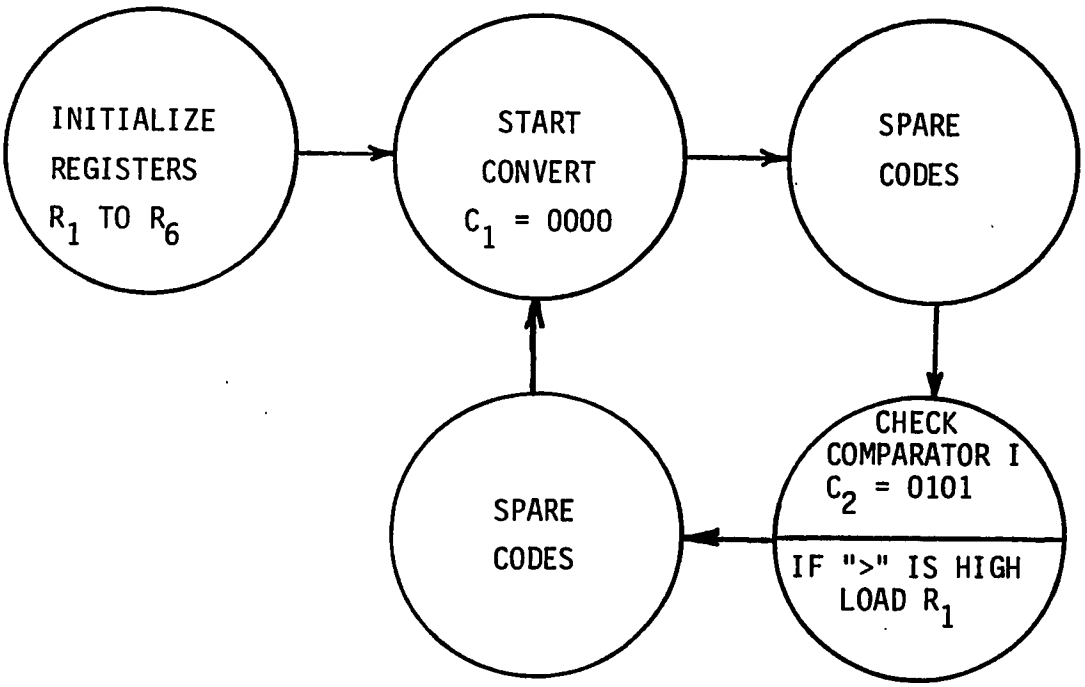
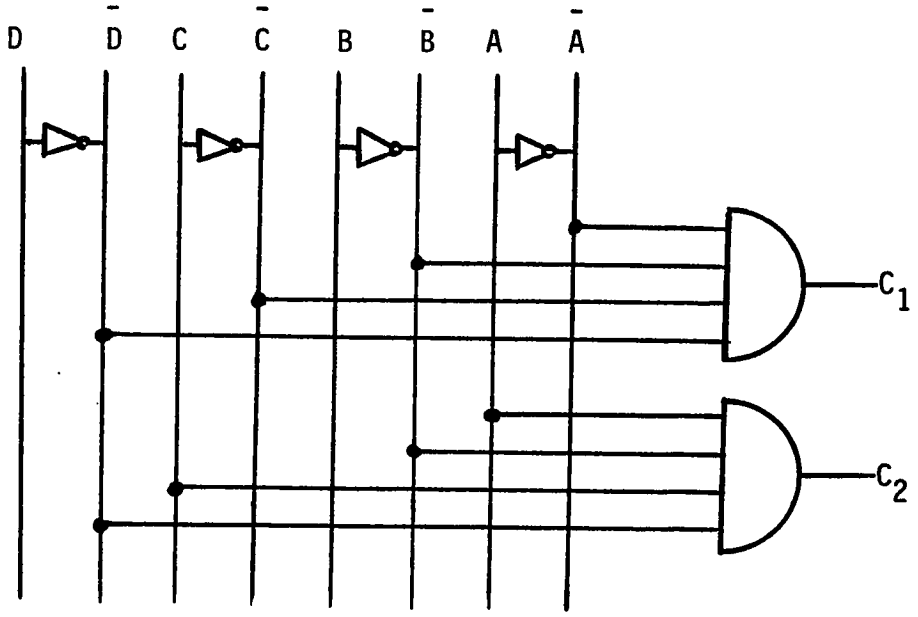


Figure 3.14. State Diagram.

TABLE V. Counting Frequencies.

Counter Outputs MSB			LSB	Time	Codes (Control signals)
D	C	B	A		
0	0	0	0	0 μs	$C_1 = \bar{D}\ \bar{C}\ \bar{B}\ \bar{A}$
0	0	0	1	62.5 μs	
0	0	1	0	125 μs	
0	0	1	1	187.5 μs	
0	1	0	0	250 μs	
0	1	0	1	312.5 μs	$C_2 = \bar{D}\ C\ \bar{B}\ A$
0	1	1	0	375 μs	
0	1	1	1	437.5 μs	
1	0	0	0	500 μs	
1	0	0	1	562.5 μs	
1	0	1	0	625 μs	
1	0	1	1	687.5 μs	
1	1	0	0	750 μs	
1	1	0	1	812.5 μs	
1	1	1	0	875 μs	
1	1	1	1	937.5 μs	
0	0	0	0	1 ms	



Where A,B,C and D are the binary counter outputs and D is the MSB.

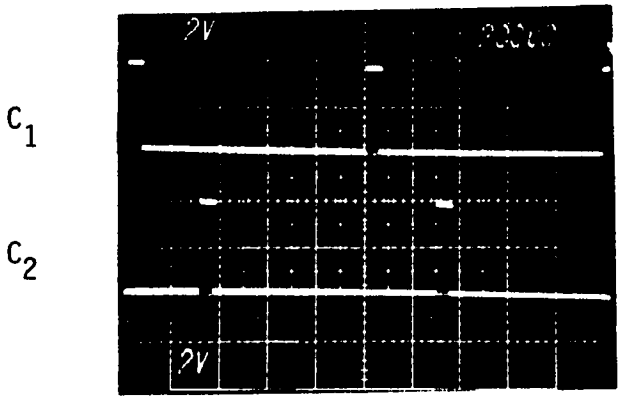


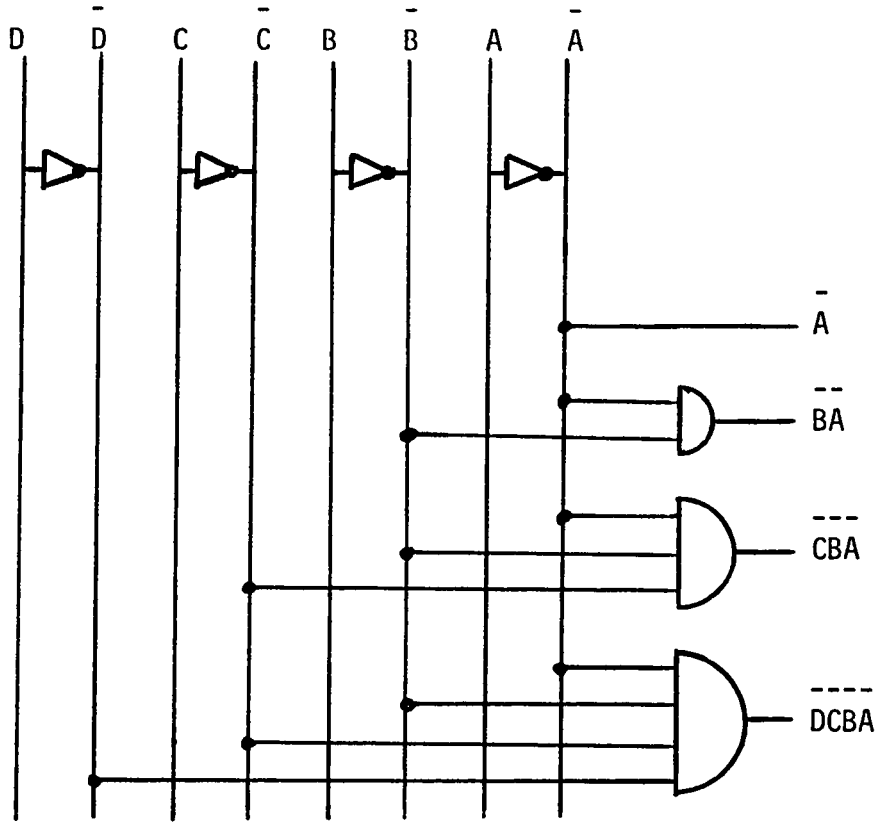
Figure 3.15. The logic diagram of the control signals C_1 and C_2 and their photocopies.

Table VI shows these division operations and the resulting frequency for a counting frequency of 1 KHZ.

The logic diagram which describes these operations is shown in Fig. 3.16. The resulting frequencies are shown in the test result section.

TABLE VI. Resulting Frequencies.

Counter Outputs				Operation	Code	Resulting frequency, CK_2.
D	C	B	A			
0	0	0	0			
0	0	0	1			
0	0	1	0	DIVIDE BY 2	$\bar{A}$	500 HZ
0	0	1	1			
0	1	0	0	DIVIDE BY 4	$\bar{B}\ \bar{A}$	250 HZ
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0	DIVIDE BY 8	$\bar{C}\ \bar{B}\ \bar{A}$	125 HZ
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			
0	0	0	0	DIVIDE BY 16	$\bar{D}\ \bar{C}\ \bar{B}\ \bar{A}$	62.5 HZ



Where A,B,C, and D are the counter outputs and D is the MSB.

Figure 3.16. Logic diagram for the division operation codes.

4. TEST RESULTS

The majority of relays in modern power systems operate from the secondaries of current and potential transformers, with secondaries of 5 amperes and 120 volts respectively, rather than from series current coils or line voltage |35|.

4.1 CURRENT TRANSFORMER TESTS

An experiment was done to check the performance characteristics of the laboratory model current transformer. A one ohm resistor was connected to the secondary side of the current transformer, to facilitate the reading of the output current directly, which is equal to the secondary side voltage. Different values of primary inputs and different secondary loads were used. Figure 4.1 shows some photocopies describing different cases. It is seen from the output characteristics, that there is no serious distortion in the current waveform and the higher degree of harmonics above the third harmonic can be neglected or omitted. No pre-sampling filter is needed in this case to limit the input current signal.

4.2 CURRENT SAMPLING TESTS

A sampling rate between 16 and 24 samples per cycle were recommended |19,20|. A sampling frequency of 1 KHZ was chosen in

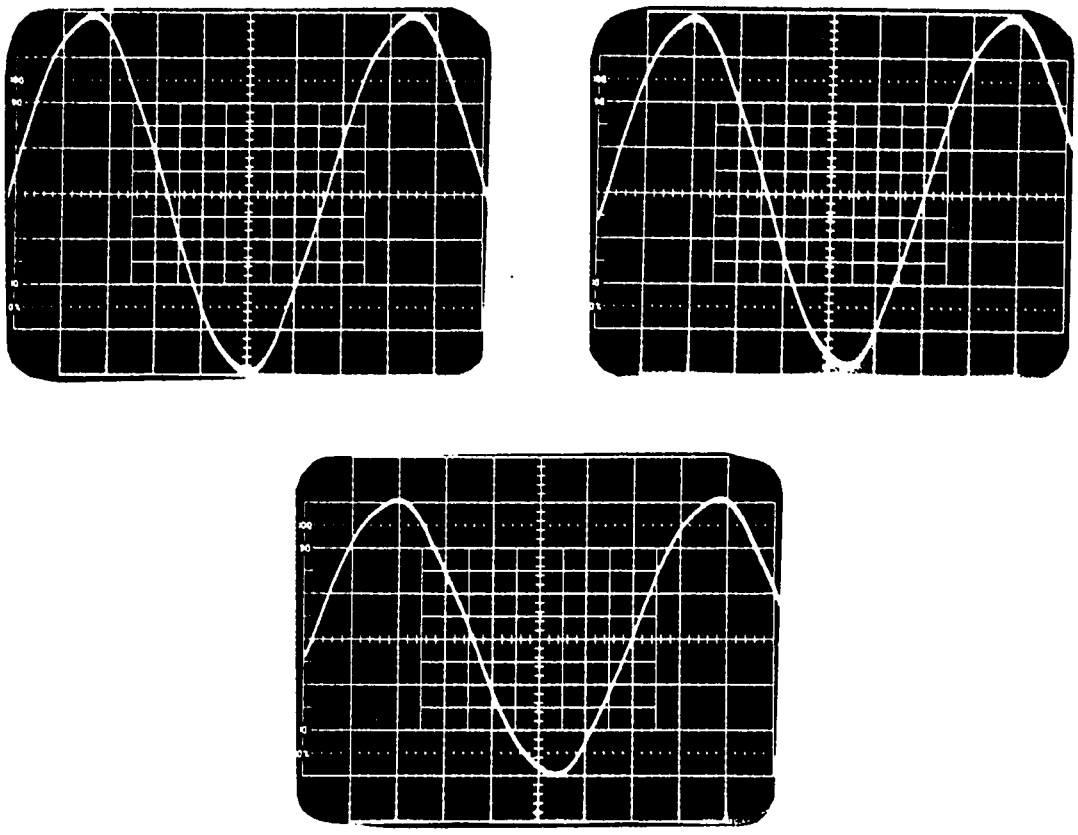


Figure 4.1. Different Current transformer outputs.

the course of this work. The dynamic range of the A/D converter is $\pm$ 5V full scale. The conversion time to reach the full scale is 200 μ sec.

An a-c input signal was fed into the analog input of the A/D converter with the start convert signal of 1 KHZ rate. At the same time a digital to analog converter was connected at the output of the analog to digital converter to display the output produced analog signal. Analog recovered signals super-imposed on the original input signals are shown in Fig. 4.2. It can be noticed that the recovered signals have the same amplitudes and frequencies as the input ones.

4.3 CHARACTERISTICS OF THE HARDWARE DIGITAL OVERCURRENT RELAY

The hardware-based digital overcurrent relay was built and tested. Its performance has been evaluated by using it to detect Overcurrents in Current Transformers mounted on circuits and feeders.

The current pick-up of the relay can be selected by means of the preset values in the registers R_2 to R_6. The shapes of these characteristics can be chosen arbitrarily by choosing the suitable values of the output logic functions of decoders f_{11} to f_{55} and by choosing the corresponding preset values in the registers R_2 to R_6. The different time-current characteristics curves can be obtained by choosing the contents of registers R_2 to R_6 as 1.25, 5, 10, 20, and 40 times the full load current respectively.

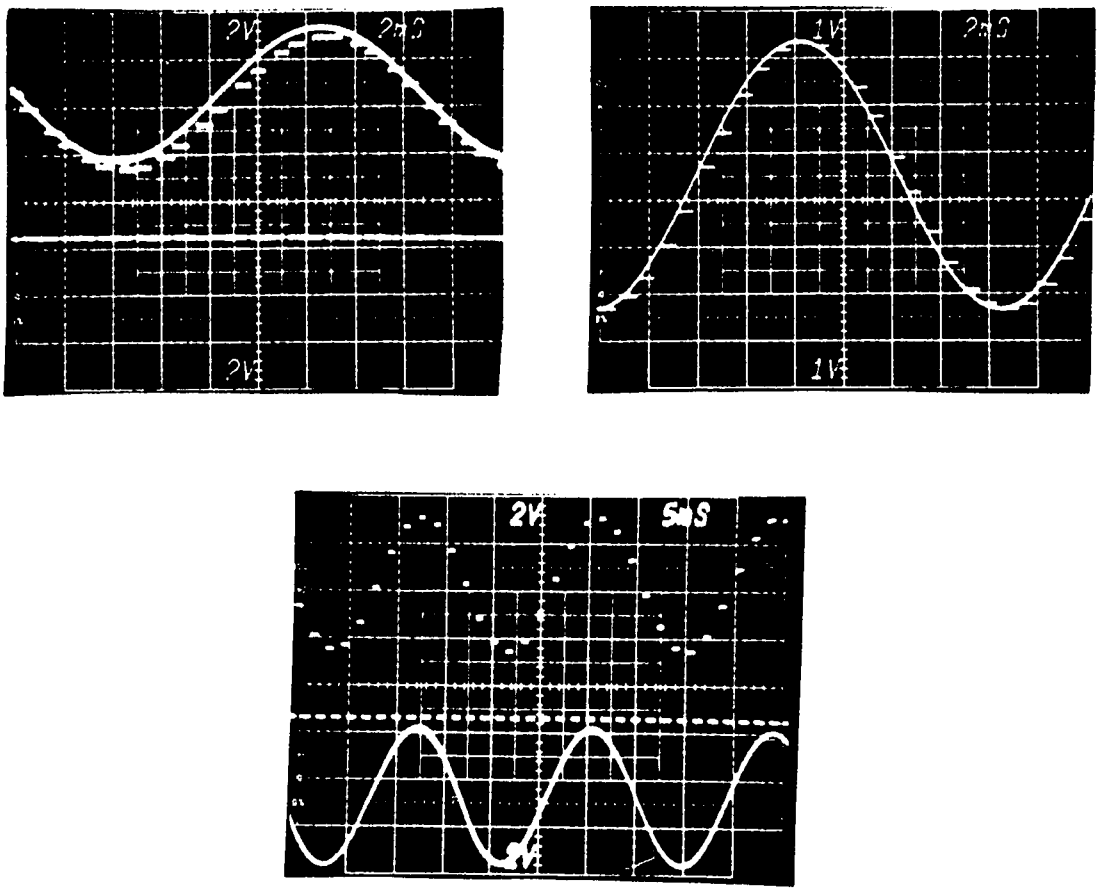


Figure 4.2. Input Current Wave forms of the Current Transformer and sampled current.

Moreover, shifting from one characteristic curve to another curve can be achieved by choosing the suitable counting frequency, CK2, which is analogous to the Time Dial Setting in the conventional relays.

A fault simulation was performed on the laboratory model to draw these characteristic curves and to check the validity of the relay. Figure 4.3 shows the connection diagram of the circuit used.

Table 4.1 shows the contents of the preset values in registers R_2 to R_6 for one sample curve, taking the counting frequency, CK2 as 1 KHZ. The associated time delays chosen are also shown in Table VII. The operation of the relay and the short circuit currents are traced using a trace recorder. The comparator response before the delay units is recorded as shown in Fig. 4.4.

Values of different short circuit currents with respect to normal currents can furnish the different operating points on the time-current characteristic curves. Figure 4.5 (a,b) shows a short circuit current value of 1.25 times the full load current. The relay operates after 16 cycles which corresponds to 255 m sec, since the power supply frequency is 60 HZ and the counting frequency is 1 KHZ. The first notch shows the relay operation. Other operating points for 5, 10, 20, and 40 times

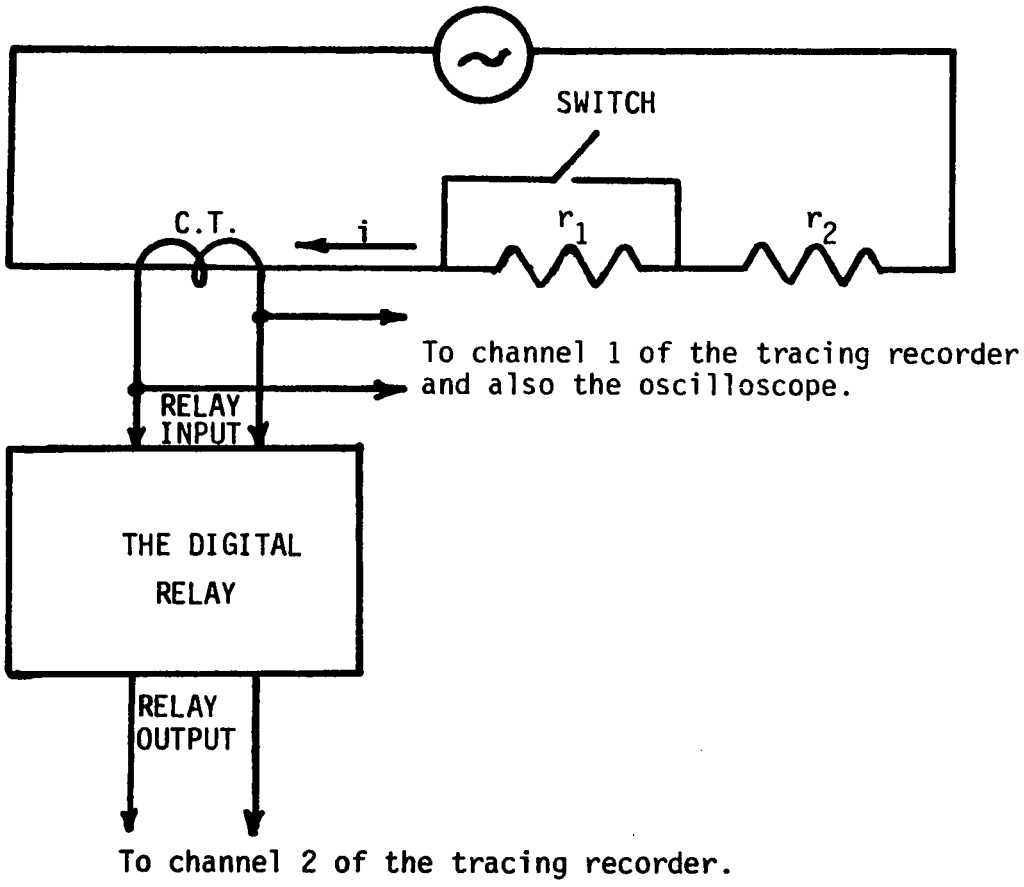


Figure 4.3. Connection Diagram of the Circuit used for fault simulation.

TABLE VII. The Contents of Registers R_2 to R_6 and the Associated Time-Delays.

$I_{F.L}$	I_f	$I_f/I_{F.L}$	The Time-Delay
$\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$	$R_2 = \bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$		$f_{55} = \bar{L}\bar{K}\bar{J}\bar{I}$ HGFE DCBA
1010 1000	= 1011 0010	1.25	= 0000 1111 1111
1.5625A	= 1.95312A		= 255
$\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$	$R_3 = \bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$		$f_{44} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$
1000 0110	= 1001 1110	5	= 0000 0101 1100
0.234375A	= 1.1718A		= 92
HGFE DCBA	$R_4 = \bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$		$f_{33} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$
1000 0100	= 1010 1000	10	= 0000 0011 1110
0.15625A	= 1.5625A		= 62
$\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$	$R_5 = \bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$		$f_{22} = \bar{L}\bar{K}\bar{J}\bar{I}$ $\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$
1000 0011	= 1011 1100	20	= 0000 0010 1101
0.1171875A	= 2.34375A		= 45
$\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$	$R_6 = \bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$		$f_{11} = LKJI$ $\bar{H}\bar{G}\bar{F}\bar{E}$ $\bar{D}\bar{C}\bar{B}\bar{A}$
1000 0010	= 1101 0000	40	= 0000 0010 0110
0.078135A	= 1.5625A		= 38

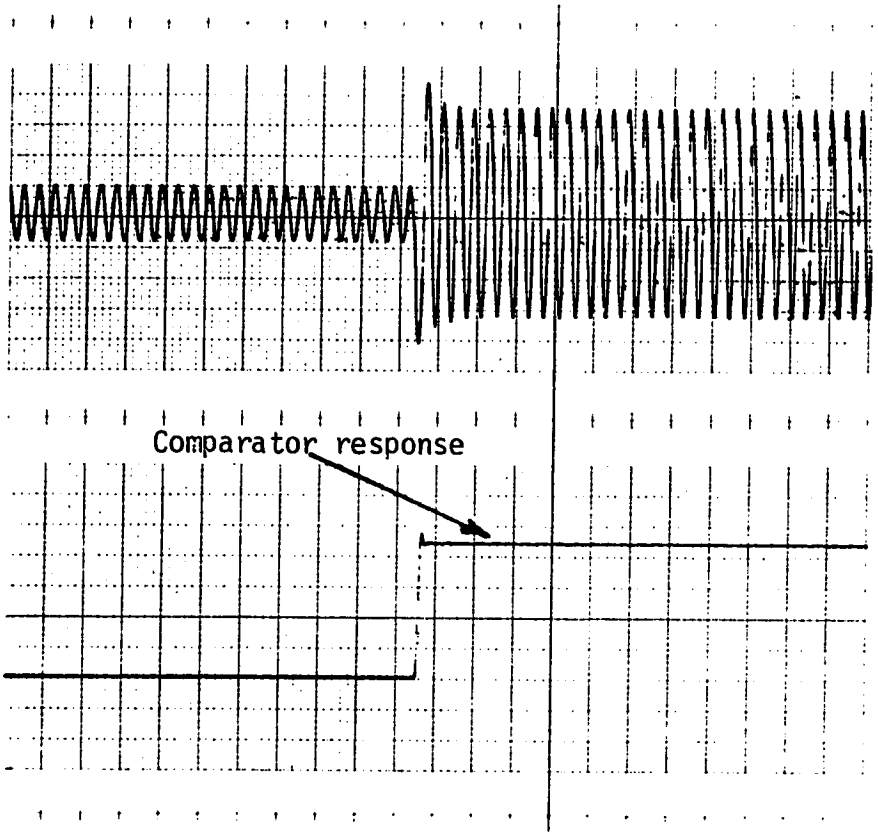


Figure 4.4. The current waveform before and after the fault and comparator III output at the instance of the fault.

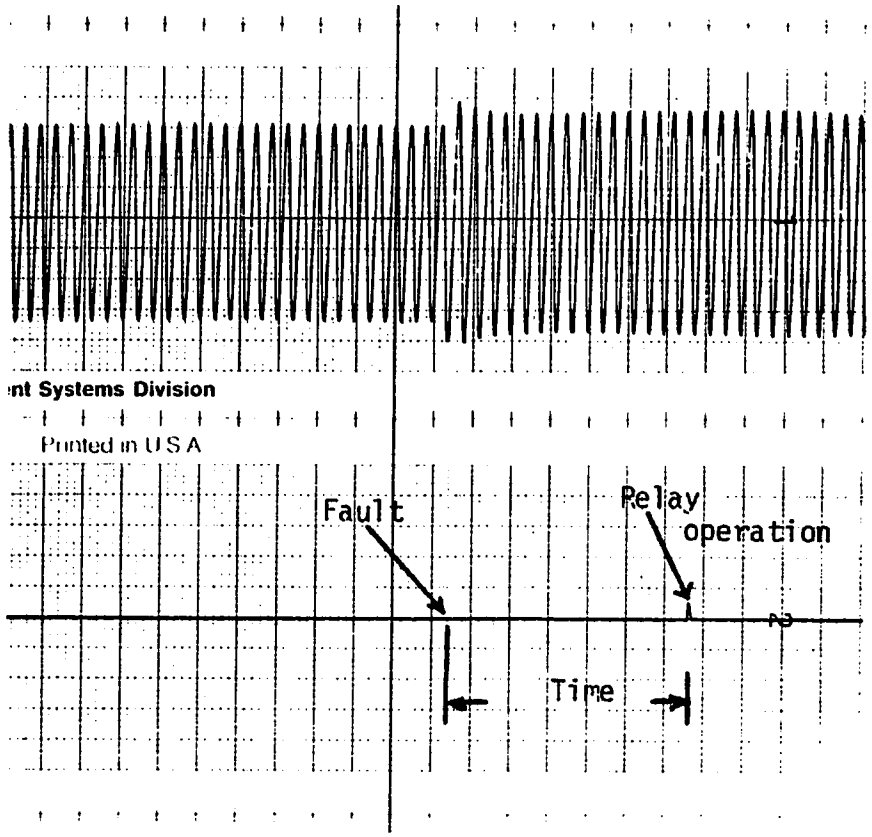


Figure 4.5(a). The current waveform in the case of 1.25 The full load current and the relay operation.

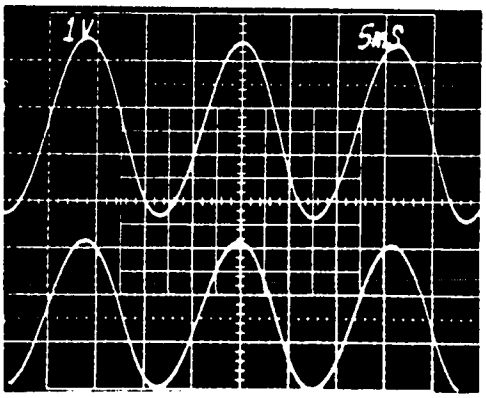


Figure 4.5(b). The steady state currents before and after the fault in the case of 1.25 the full load current.

full load currents are shown in Figs. 4.6 to 4.9 respectively.

The relay will operate after 5.5 cycles, or a delay of 92 m sec, in the case of 5 times, after 3.75 cycles, or a delay of 62 m sec, in the case of 10 times, after 2.75 cycles, or a delay of 45 m sec, in the case of 20 times, and after 2.25 cycles, or a delay of 38 m sec in the case of 40 times.

Plotting these different points on a log-log paper gives one sample characteristic curve of the relay as shown in Fig. 4.10.

Some adjustments have been made to obtain results for Inverse, Very Inverse, Extremely Inverse, Short-time, Long-time and definite time characteristics. Only one relay with different settings can give all these characteristics available from more than one conventional relay. Table VIII shows the relation between the counting frequency and the time dial setting numbers. The time dial settings could be the outputs of a frequency divider. The logic functions f_{11} to f_{55} for the different types of relays are chosen as shown in Table IX. The whole set of curves for the digital over-current relay are shown in Fig. 4.11.

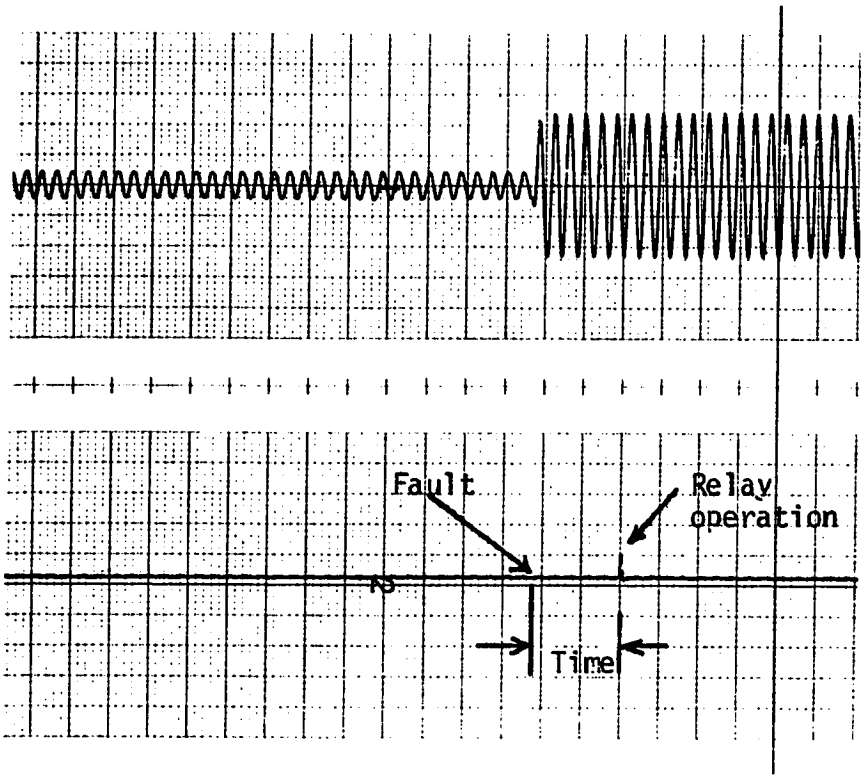


Figure 4.6(a). The current waveform in the case of 5 The full load current and the relay operation.

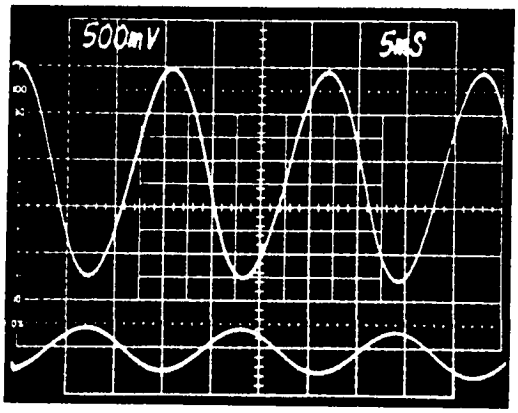


Figure 4.6(b). The steady state currents before and after the fault in the case of 5 the full load current.

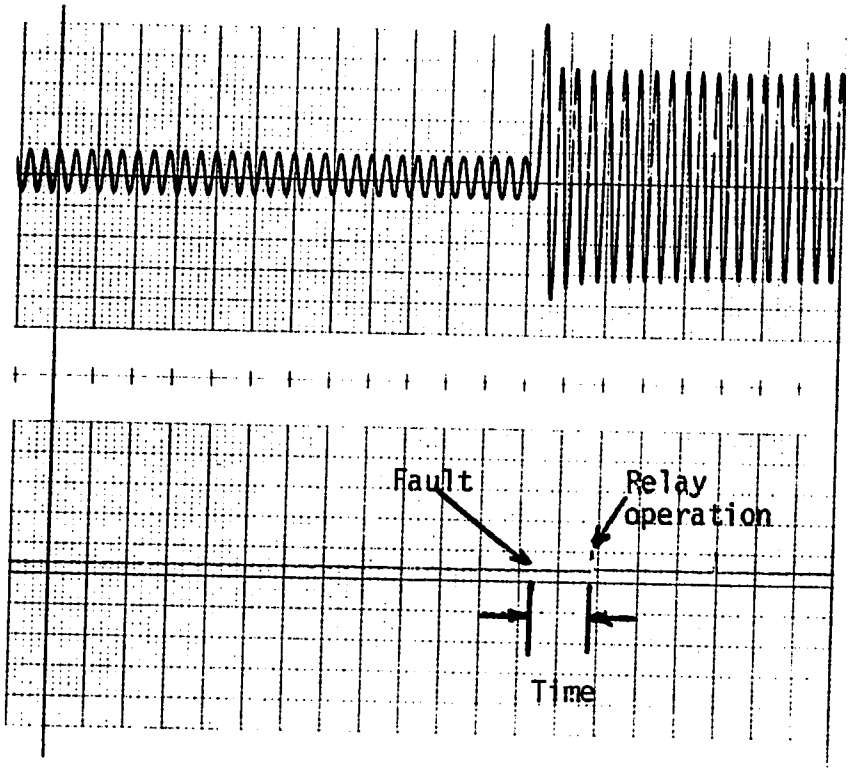


Figure 4.7(a). The current waveform in the case of 10 the full load current and the relay operation.

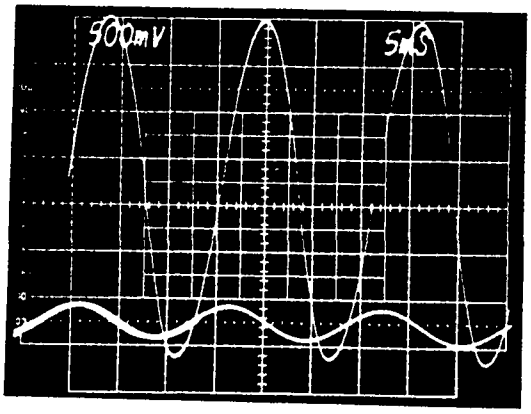


Figure 4.7(b). The steady state currents before and after the fault in the case of 10 the full load current.

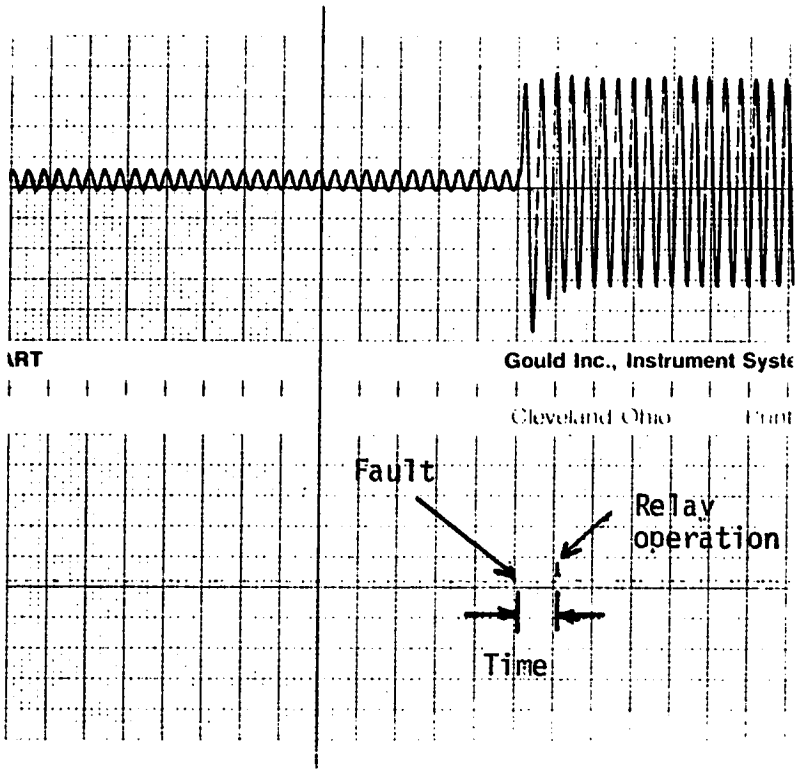


Figure 4.8(a). The current waveform in the case of 20 the full load current and the relay operation.

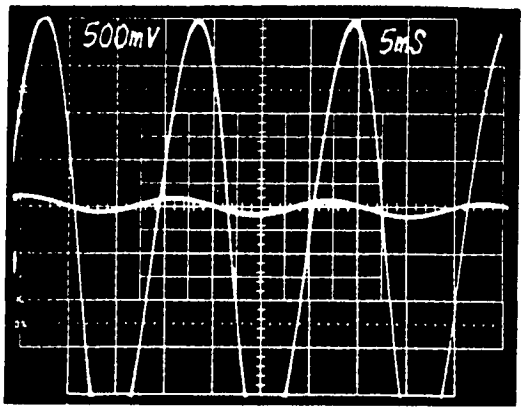


Figure 4.8(b). The steady state currents before and after the fault in the case of 20 the full load current.

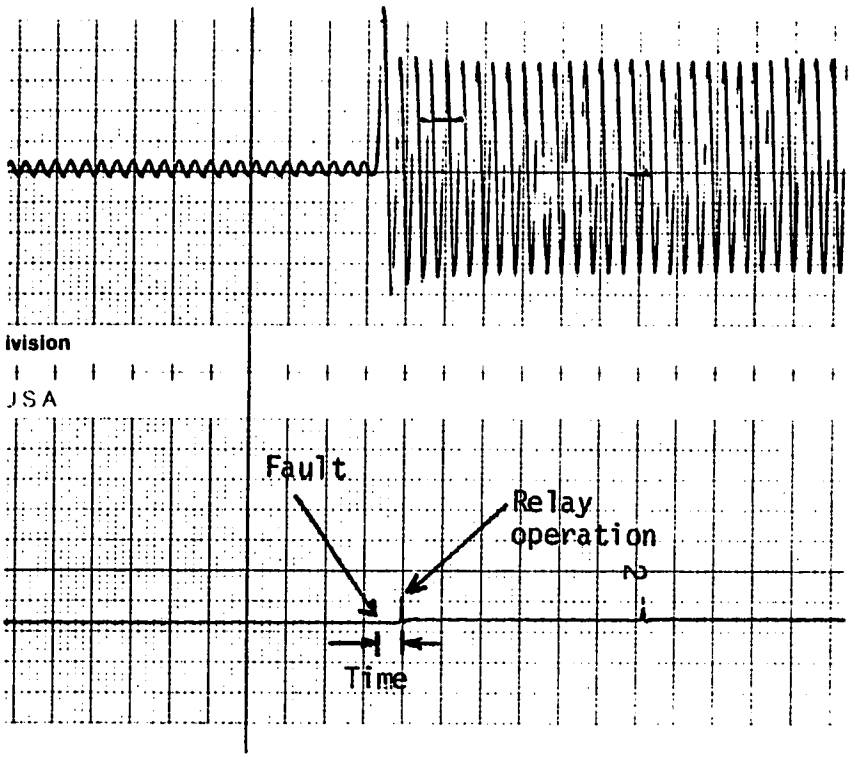


Figure 4.9(a). The current waveform in the case of 40 the full load current and the relay operation.

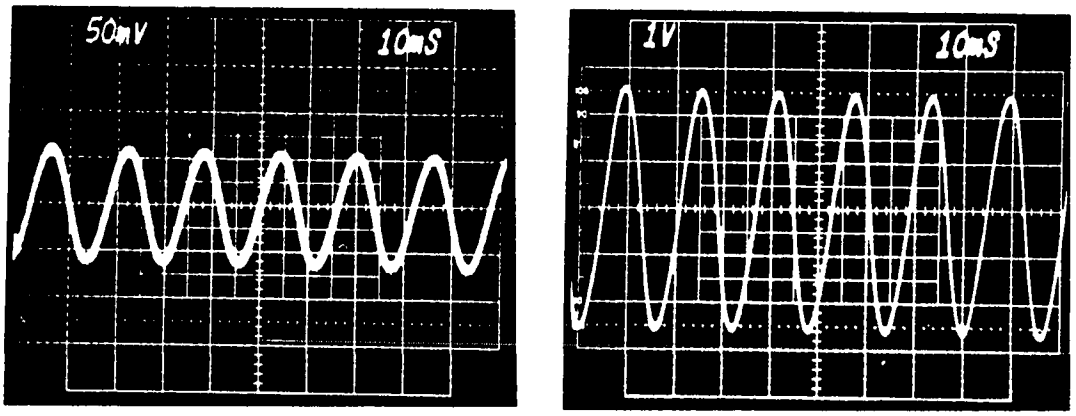


Figure 4.9(b). The steady state currents before and after the fault in the case of 40 the full load current.

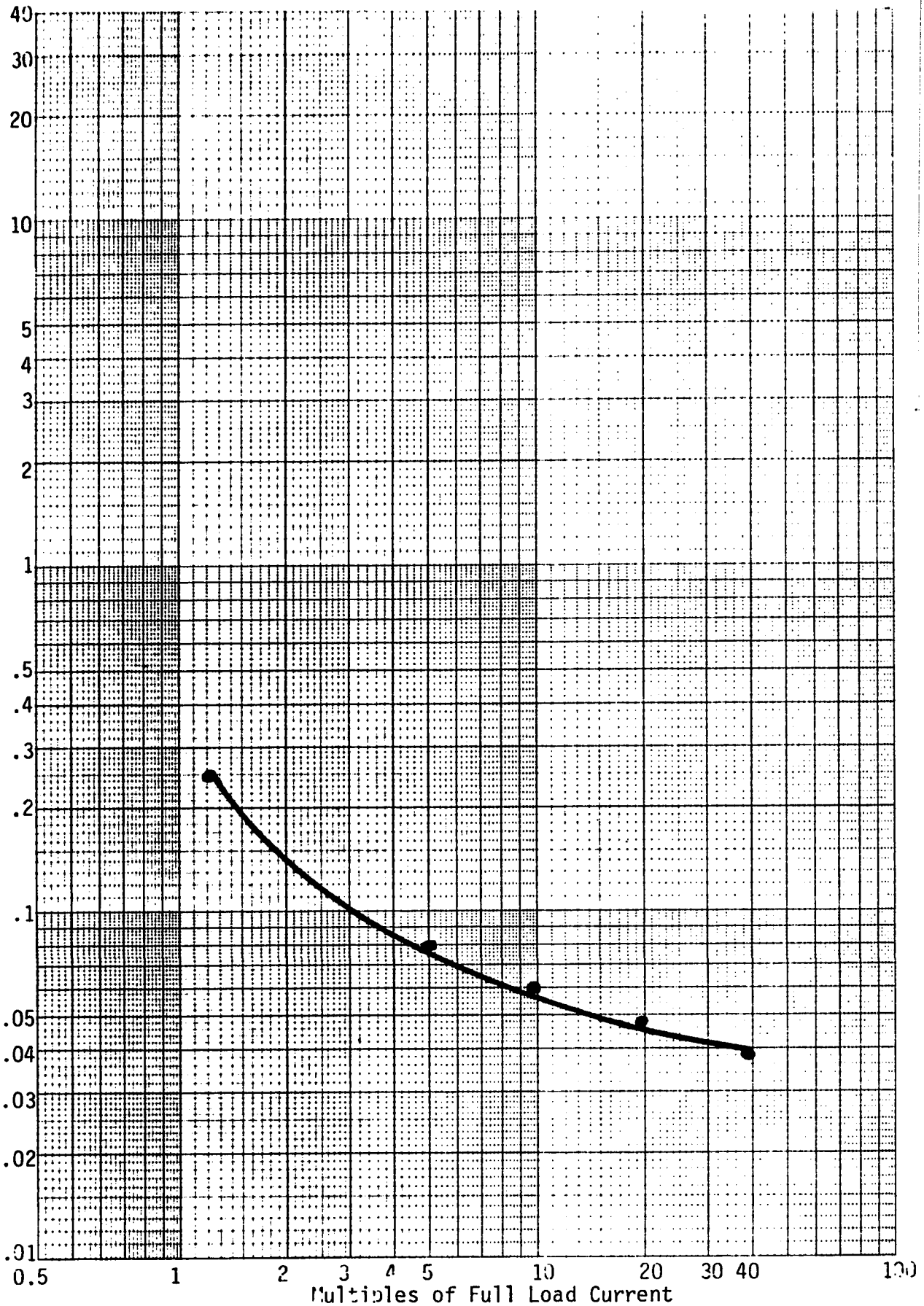


Figure 4.10. Time-Current Characteristic curve of the digital relay.

TABLE VIII. Time Dial Settings and Counting Frequencies.

Counting frequency, CK2	Time dial settings
1000 HZ	1
500 HZ	2
200 HZ	3
100 HZ	4
50 HZ	5
25 HZ	6
10 HZ	7

TABLE IX. Logic Functions for the Different Types of Relays.

Logic Functions	Inverse Relay Code			Very Inverse Relay Code			Extreme Inverse Code		
	----	----	--	----	----	- -	----	----	- -
f_{55}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	----	----	----		----	----	--
f_{44}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	- -	----	---	- -	----	---	- --
f_{33}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	-- -	----	----	-- -	- --	----	--	-- -
f_{22}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	--	- -	- -	----	-	- -	--
f_{11}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA

Logic Functions	Short-Time Code			Long-Time Code			Definite-Time Code		
	----	----		----	----	--	----	----	
f_{55}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	----	----	---	-- -	----	----	
f_{44}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	- --	----	-- -	- --	----	----	
f_{33}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	--	----	- --	- -	----	---	-- -
f_{22}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA
	----	---	-- -				----	- -	----
f_{11}	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA	LKJI	HGFE	DCBA

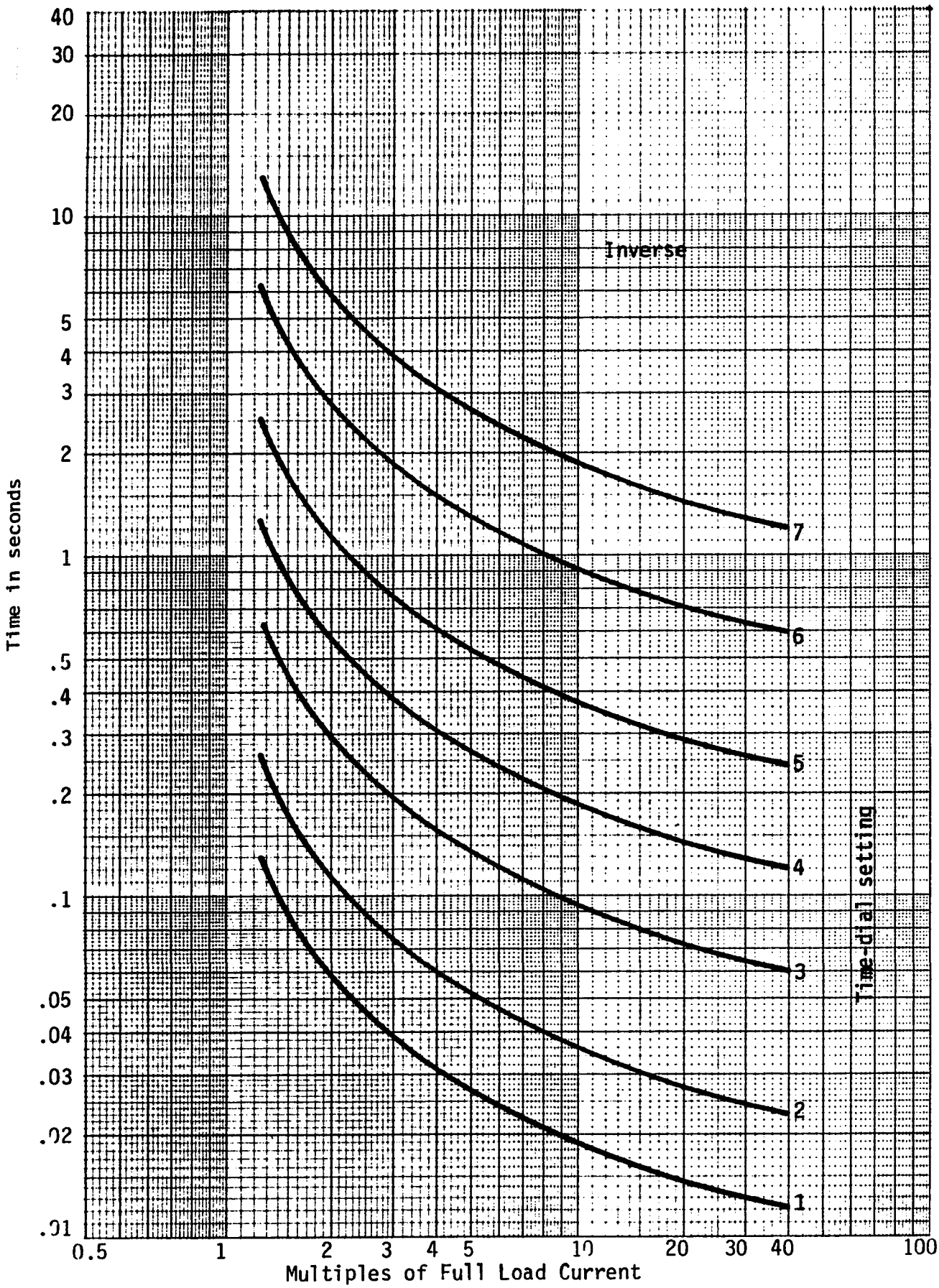


Figure 4.11. Time-Current Characteristic curves of the digital relay.

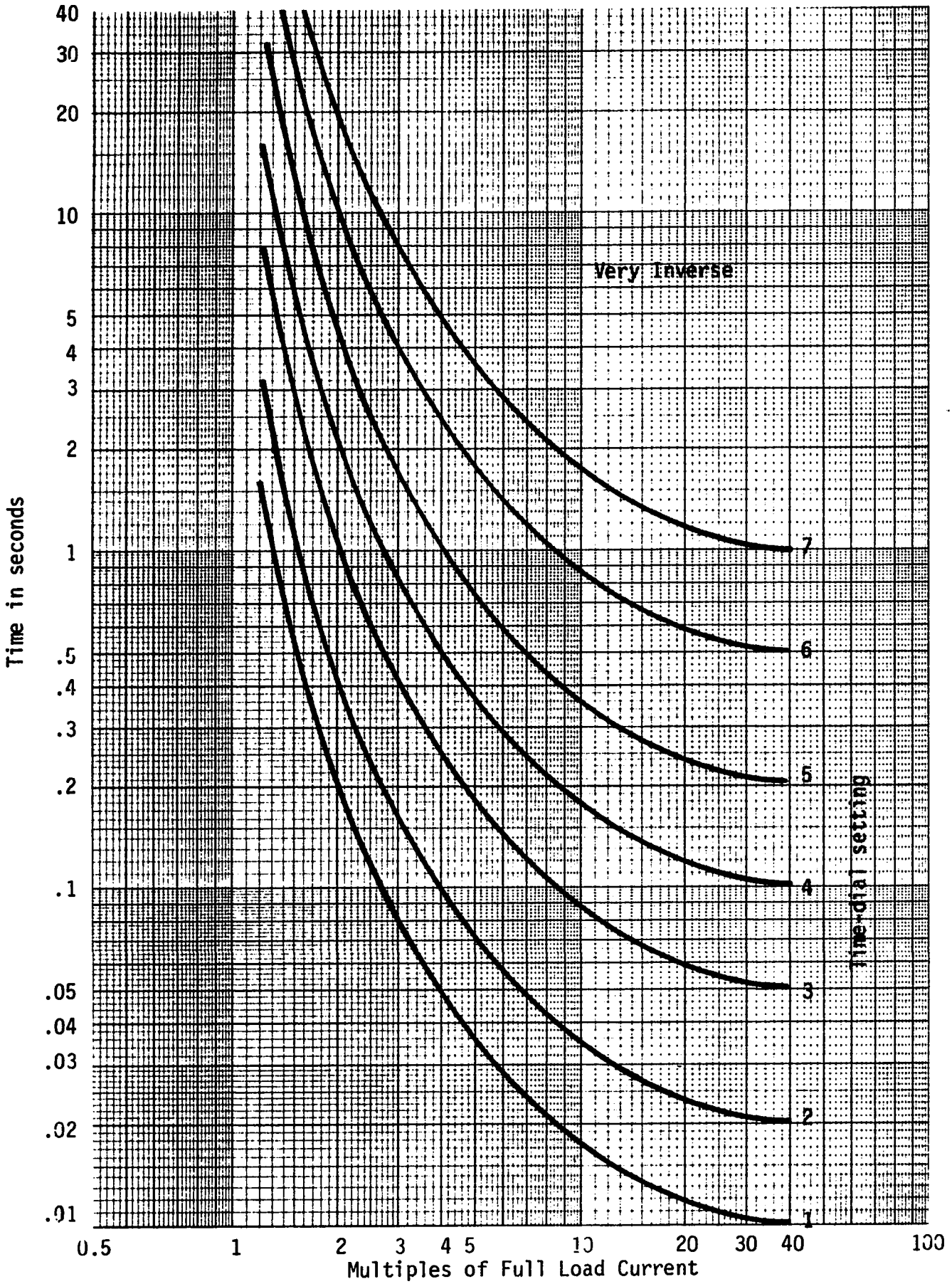


Figure 4.11. Time-Current Characteristic curves of the digital relay.

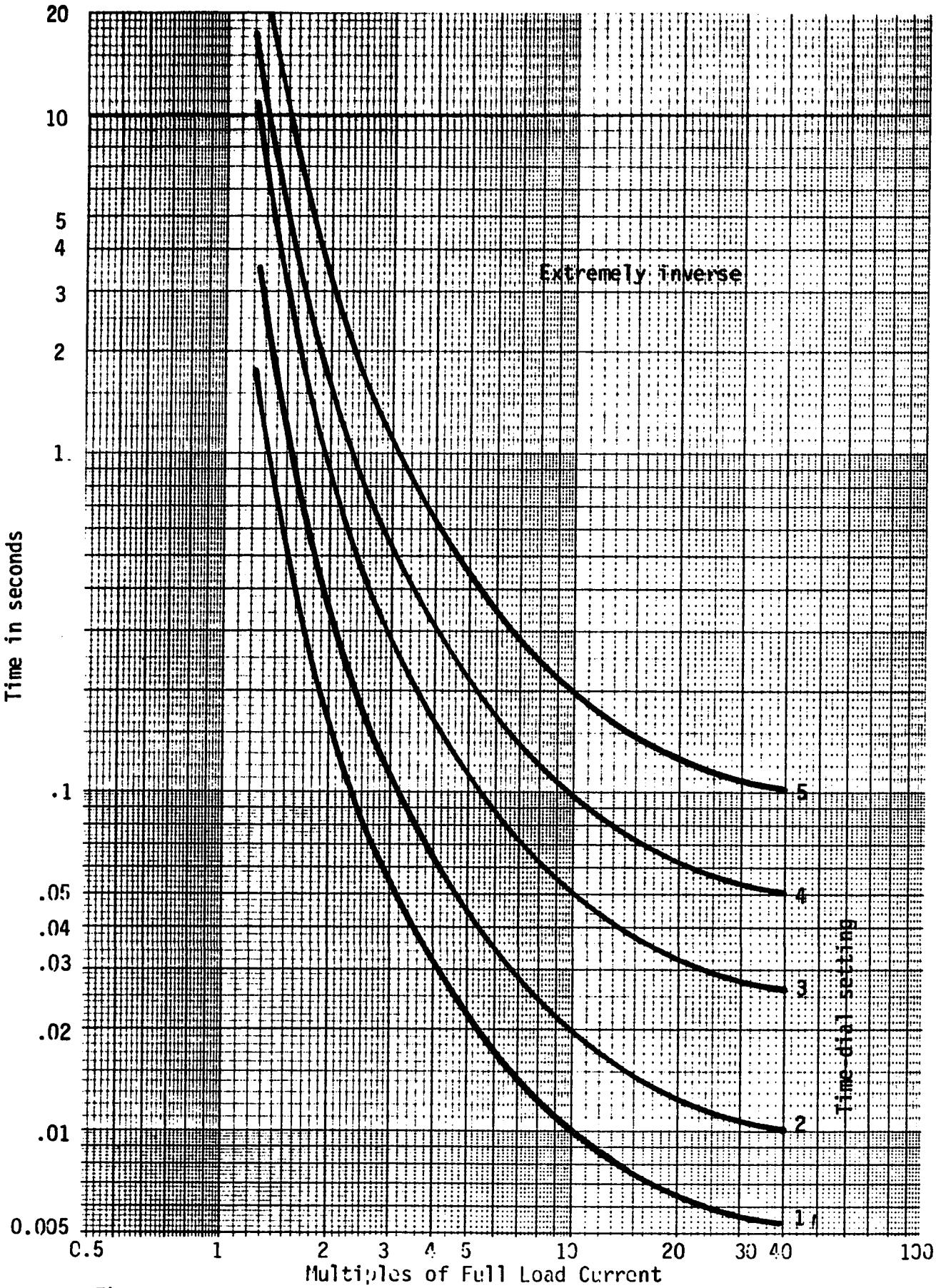


Figure 4.11. Time-Current Characteristic curves of the digital relay.

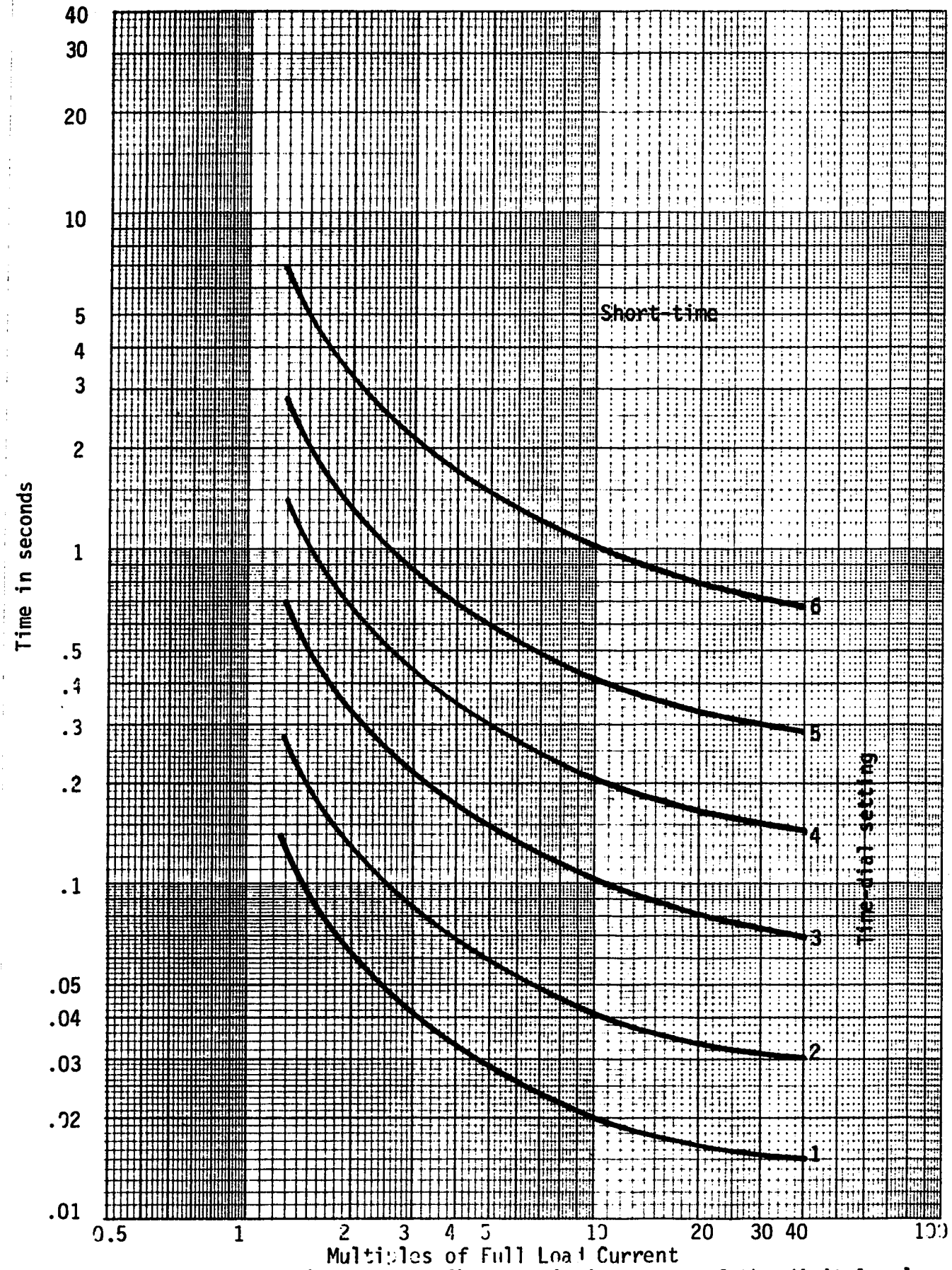


Figure 4.11. Time-Current Characteristic curves of the digital relay.

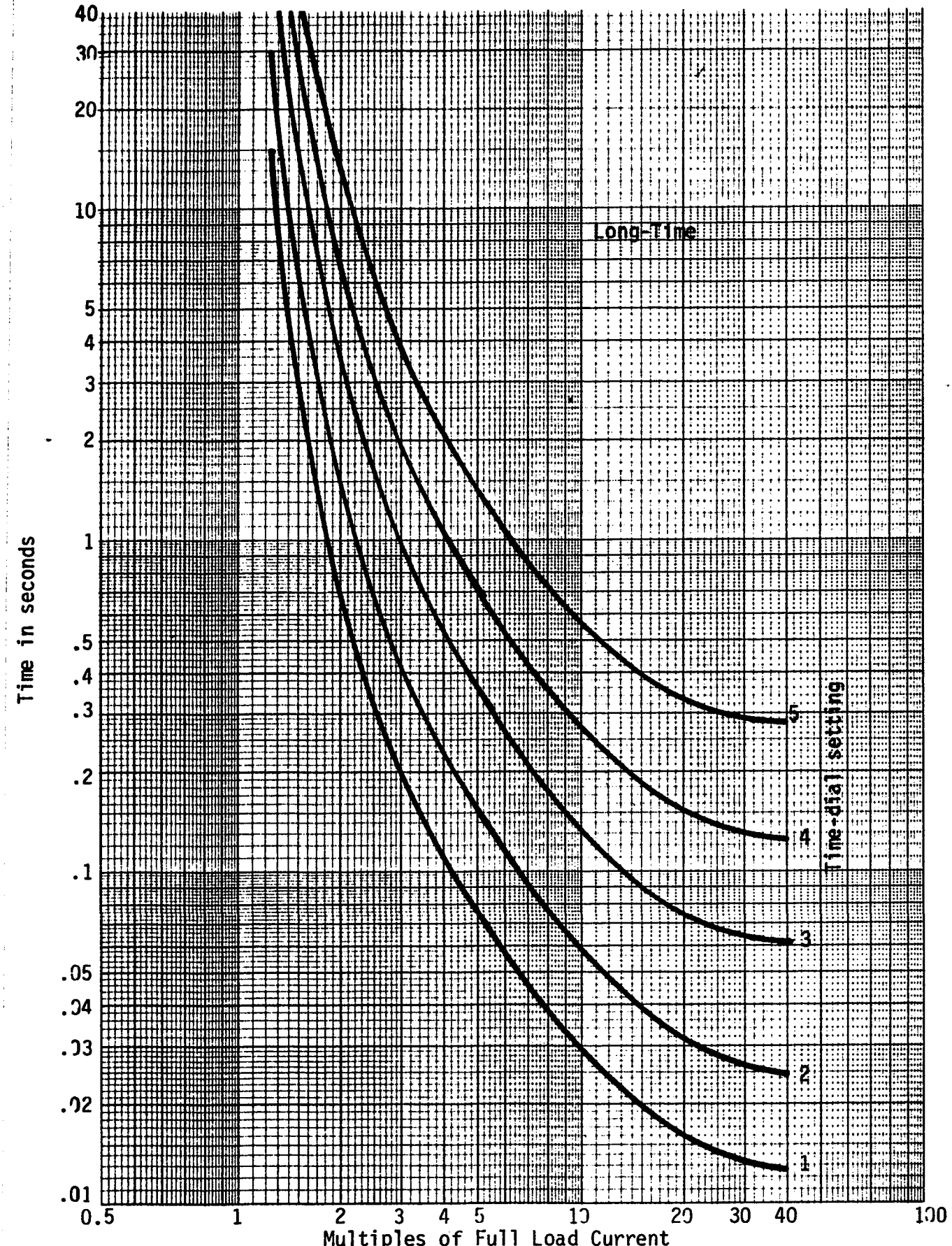


Figure 4.11. Time-Current Characteristic curves of the digital relay.

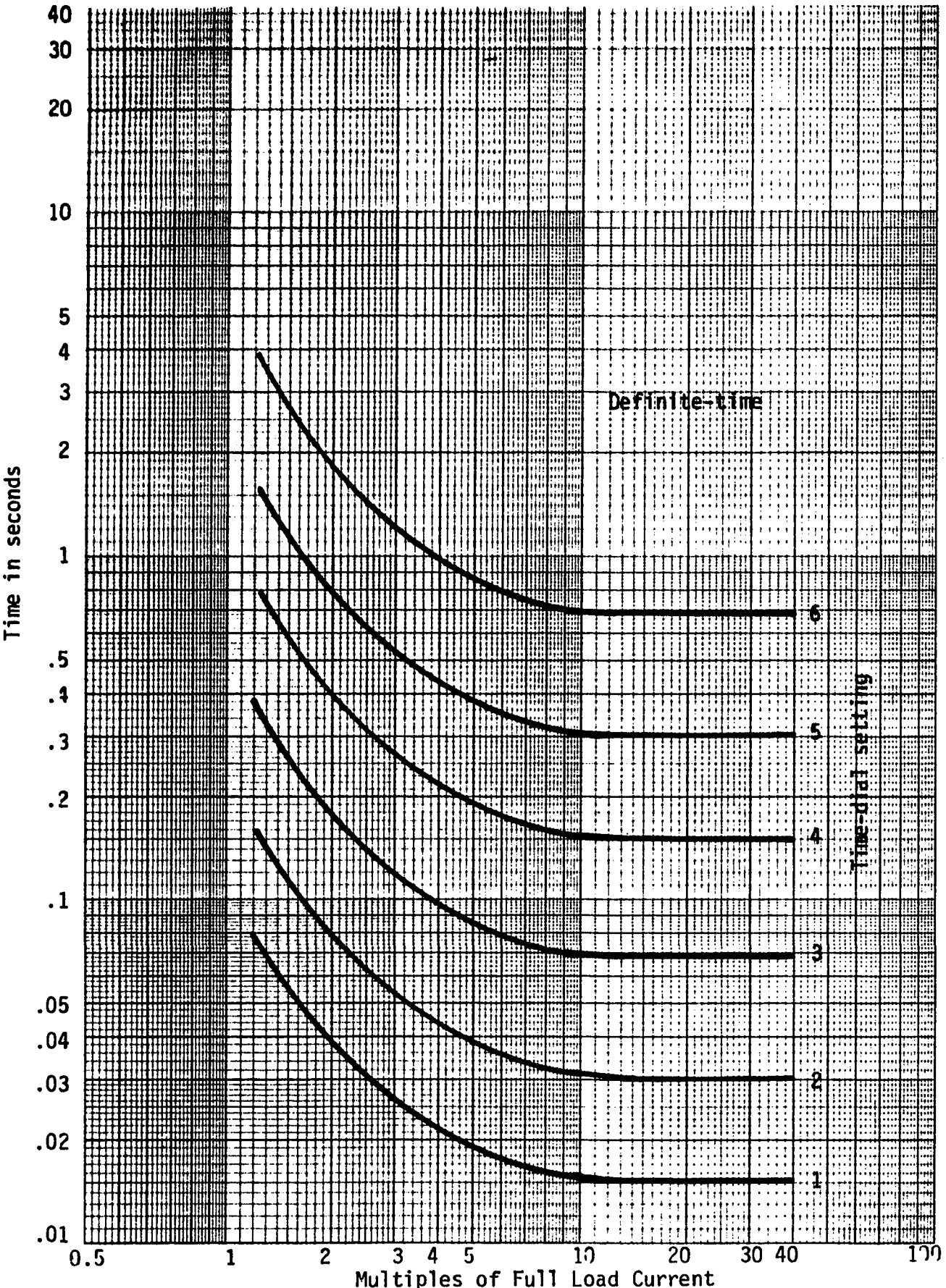


Figure 4.11. Time-Current Characteristic curves of the digital relay.

4.4 DISCUSSIONS AND COMPARISON OF THE DIGITAL HARDWARE RELAY TEST RESULTS WITH CONVENTIONAL RELAYS

The digital over-current relay time-current characteristic curves, being conventional in shape, allow for easy coordination with solid-state and induction models.

In the conventional over-current relays, variation in the operating time is accomplished by moving the time dial to a specified setting determined from a family of time-current curves supplied by the manufacturer of a particular type of relay. Most adjustable induction-type overcurrent relays have 10 or 11 time-dial position marks whose identifying numbers are arbitrarily assigned without regard to the actual operating time of the particular setting |35|. The current pick-up or the current multiples of the relay is selected by means of taps in the operating coil which are connected to receptacles in a tap plate. The family of curves for an inverse-time relay for different magnitudes of current, and time-dial settings is shown in Fig. 4.12. A similar family of curves for a very-inverse-time relay and an extremely-inverse-time relay are shown also in Fig. 4.12. The relay can be set at intermediate points between the time-dial numbered divisions, in which case their performance can be determined from interpolated time current curves.

In the solid state relays, extremely inverse and very inverse time-current characteristics have been obtained by using

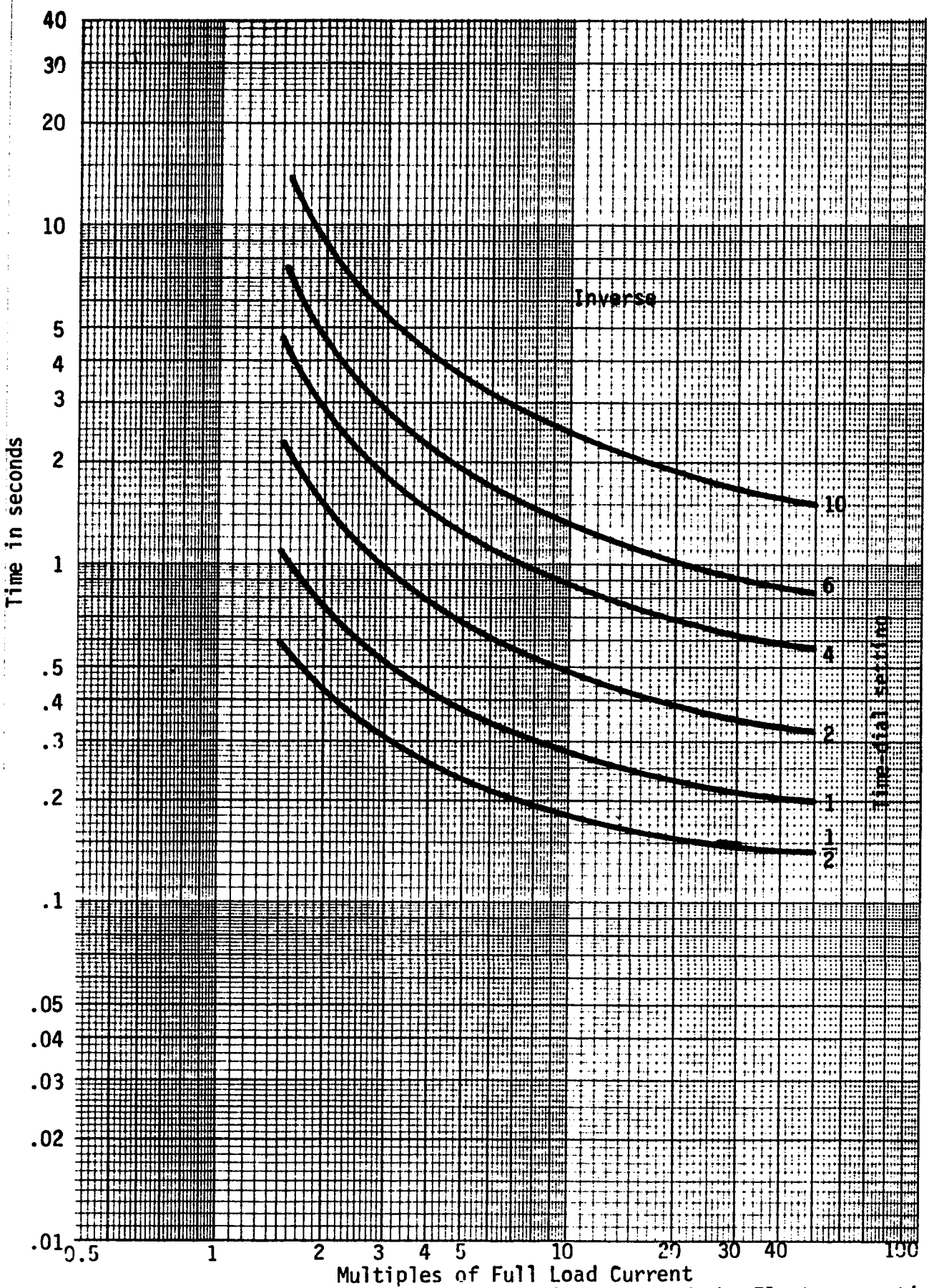


Figure 4.12. Time-Current Characteristic curves of the Electromagnetic relay.

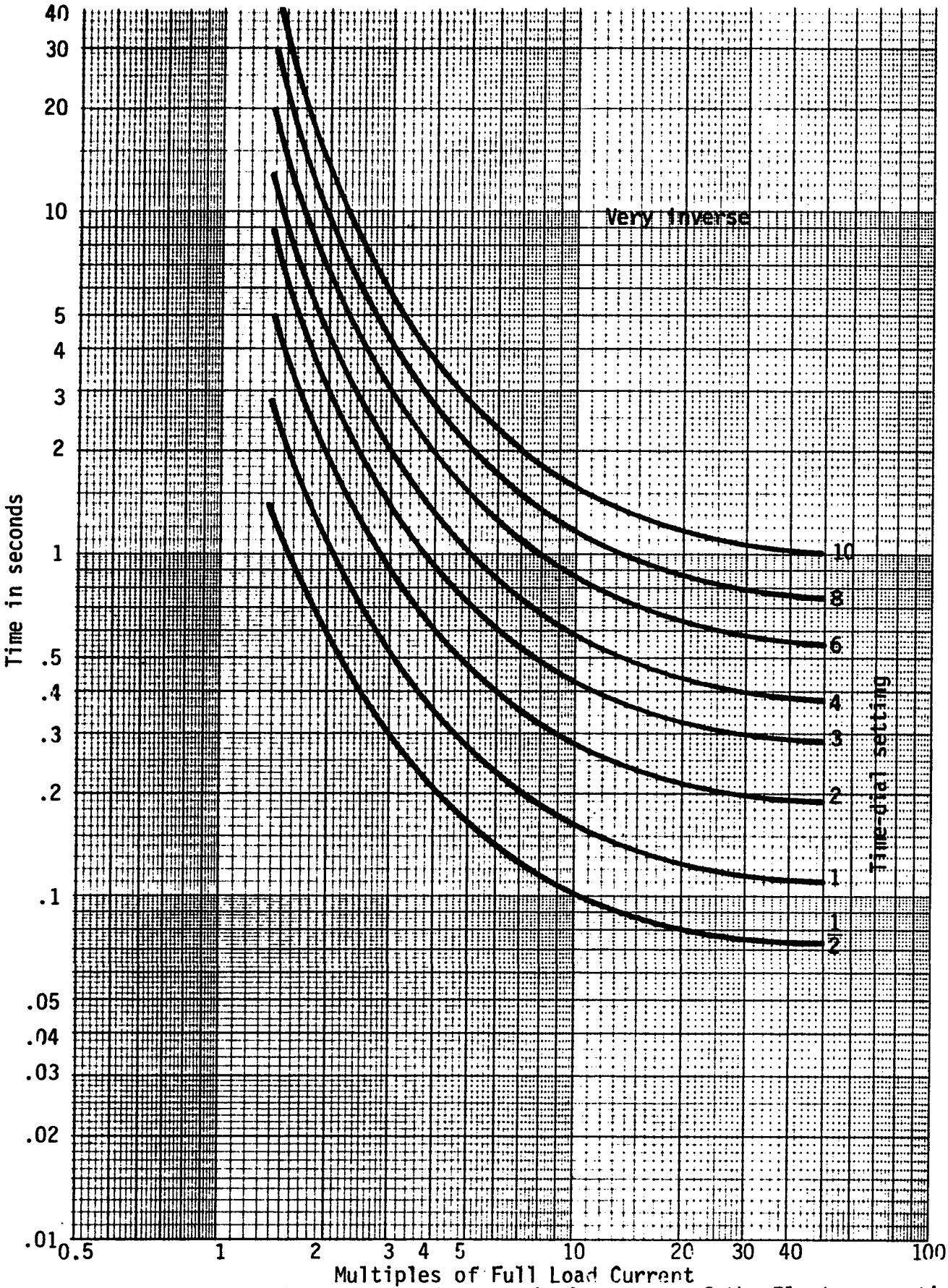


Figure 4.12. Time-Current Characteristic curves of the Electromagnetic rela

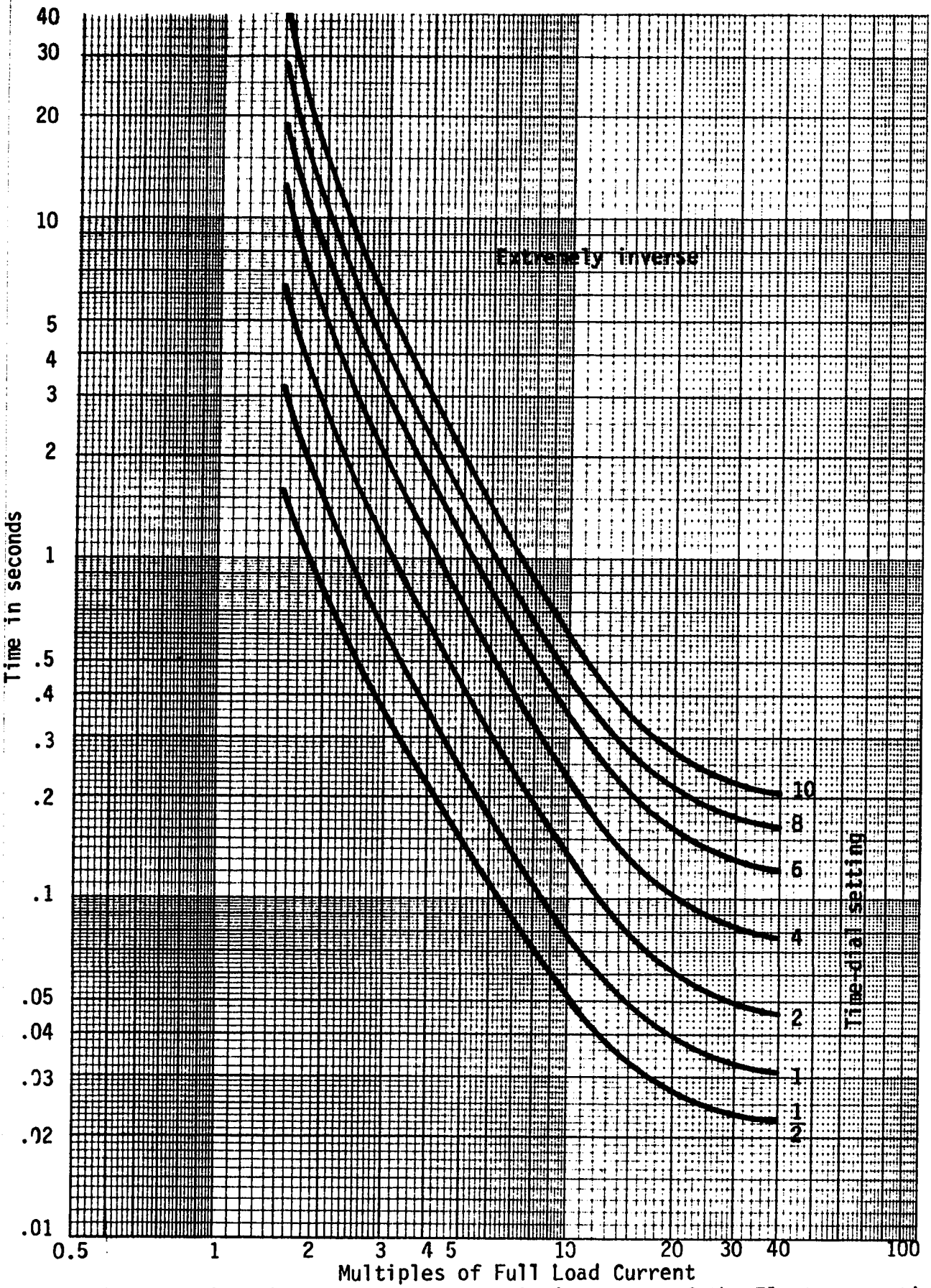


Figure 4.12. Time-Current Characteristic curves of the Electromagnetic relay.

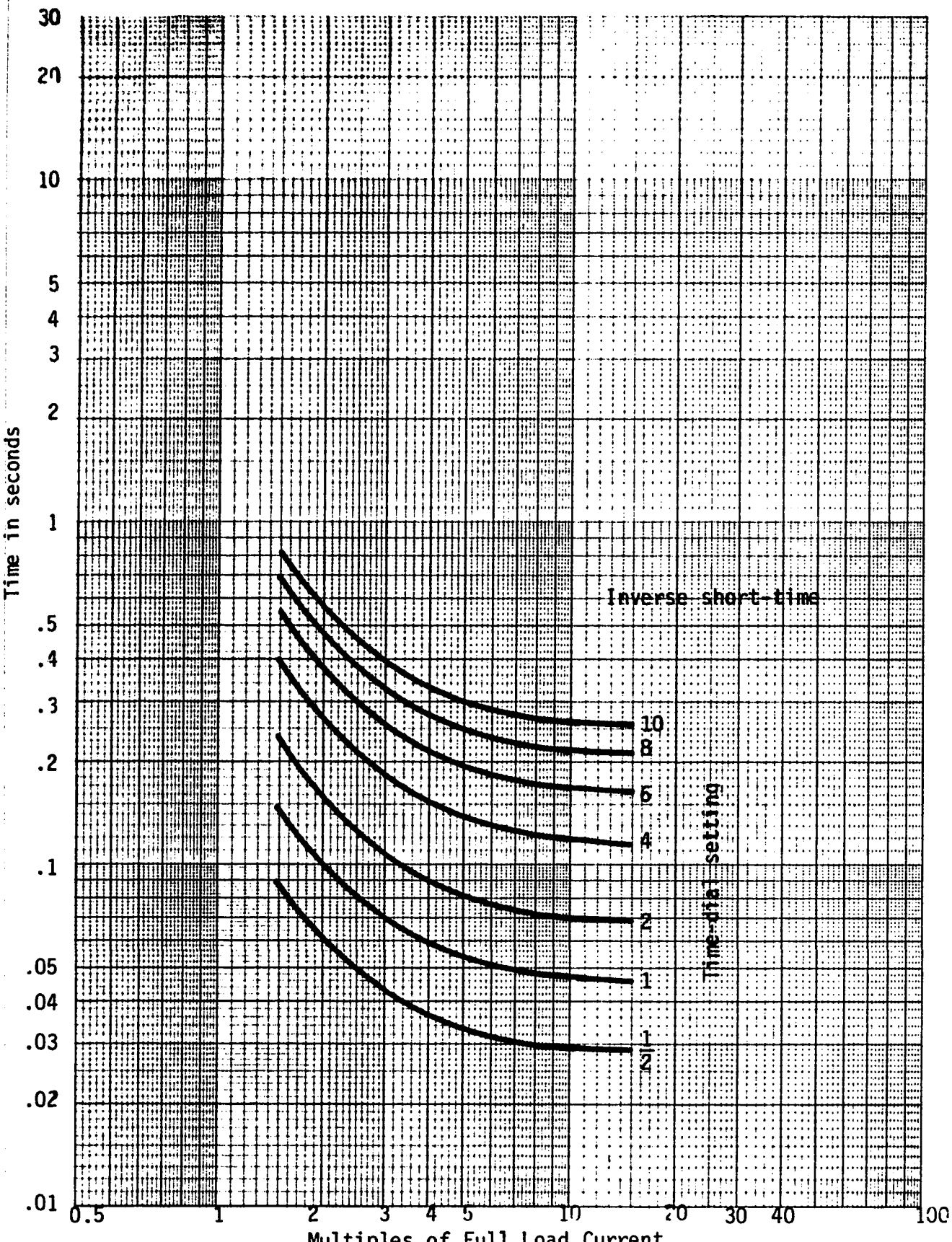


Figure 4.12. Time-Current Characteristic curves of the Electromagnetic relay.

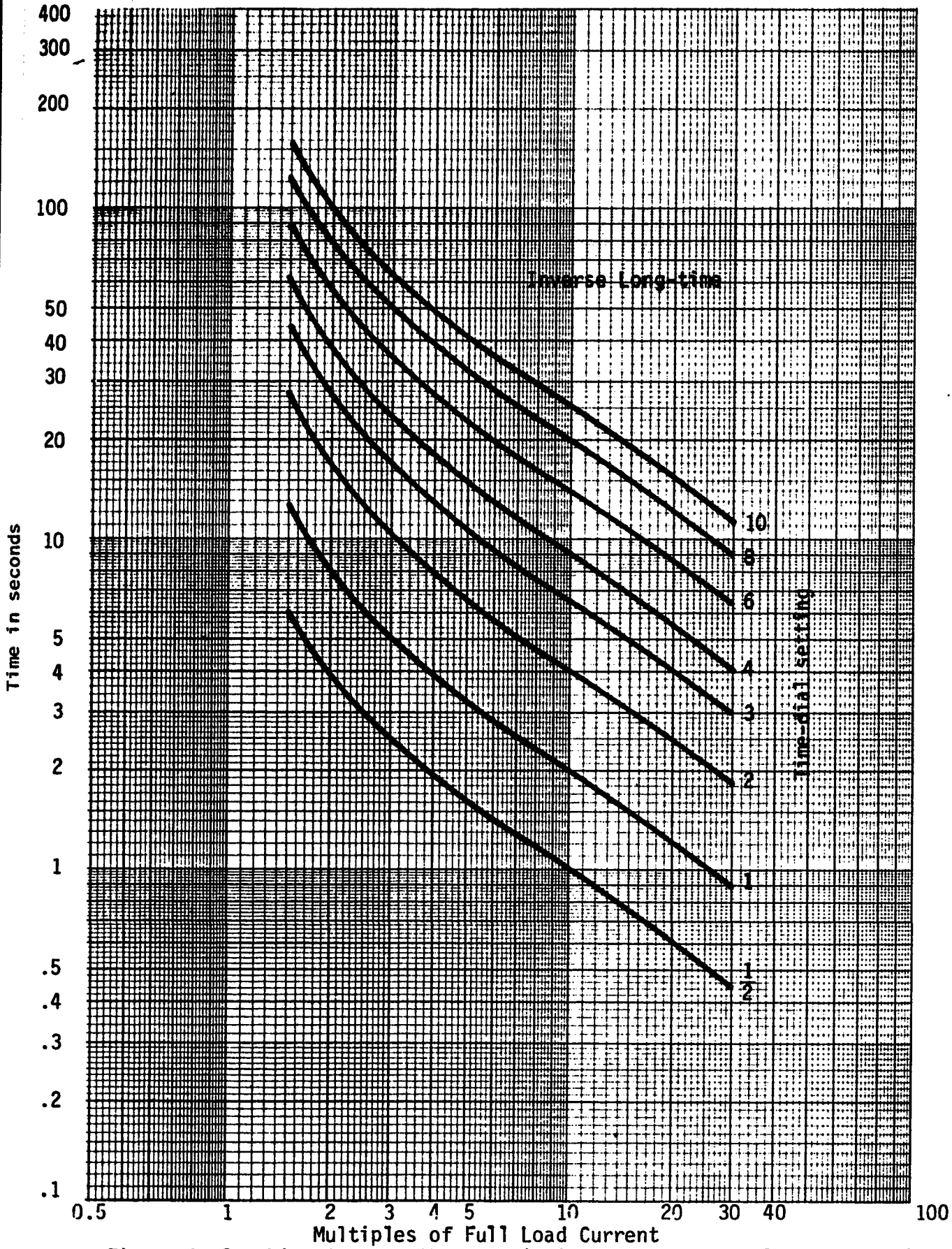


Figure 4.12. Time-Current Characteristic curves of the Electromagnetic relay.

RC timing techniques. These relays were designed with familiar time-current characteristics as shown in Fig. 4.13 |13|.

For the resetting of the relay, in solid-state overcurrent relays, timing capacitors are discharged by a switching circuit when the input current fails below the pickup. Full reset is obtained in 20 to 100 m sec depending on the time-current characteristics used. With induction relays, the succeeding reclosures are delayed in the order of 15 to 120 seconds |13|, while in the digital overcurrent relay, this can be done by sending a reset signal to the delay counters. This resetting takes 25 nano seconds. This pulse is ANDed with the actuating signal.

The inertia of mechanical relays will cause continued disk rotation after a fault current is removed. This can cause unnecessary trips or requires additional space between time curves of two cascaded relays. For example, a relay set for 0.4 seconds at a specified current having an overtravel of 0.1 seconds will trip if the fault lasts 0.3 seconds. Solid-state relays have negligible overtravel and allow closer coordination |13|. The Digital relays have no overtravel and allow more closer coordination.

Generally, the digital relays have been designed with traditional curve-shapes such as inverse, very inverse, extremely inverse, definite time, and short time, for easy coordination with solid-state relays, electro-mechanical relays and fuses.

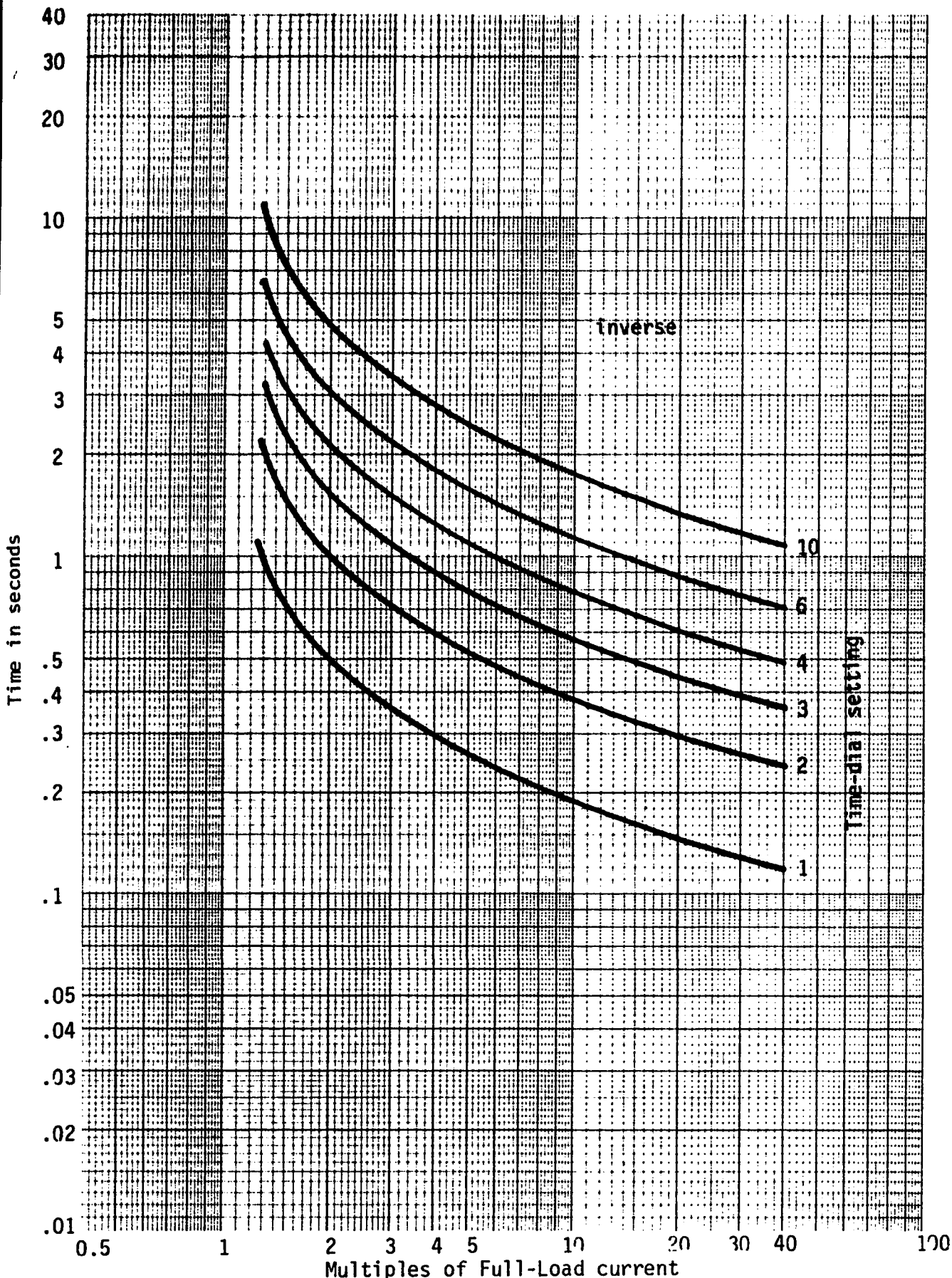


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

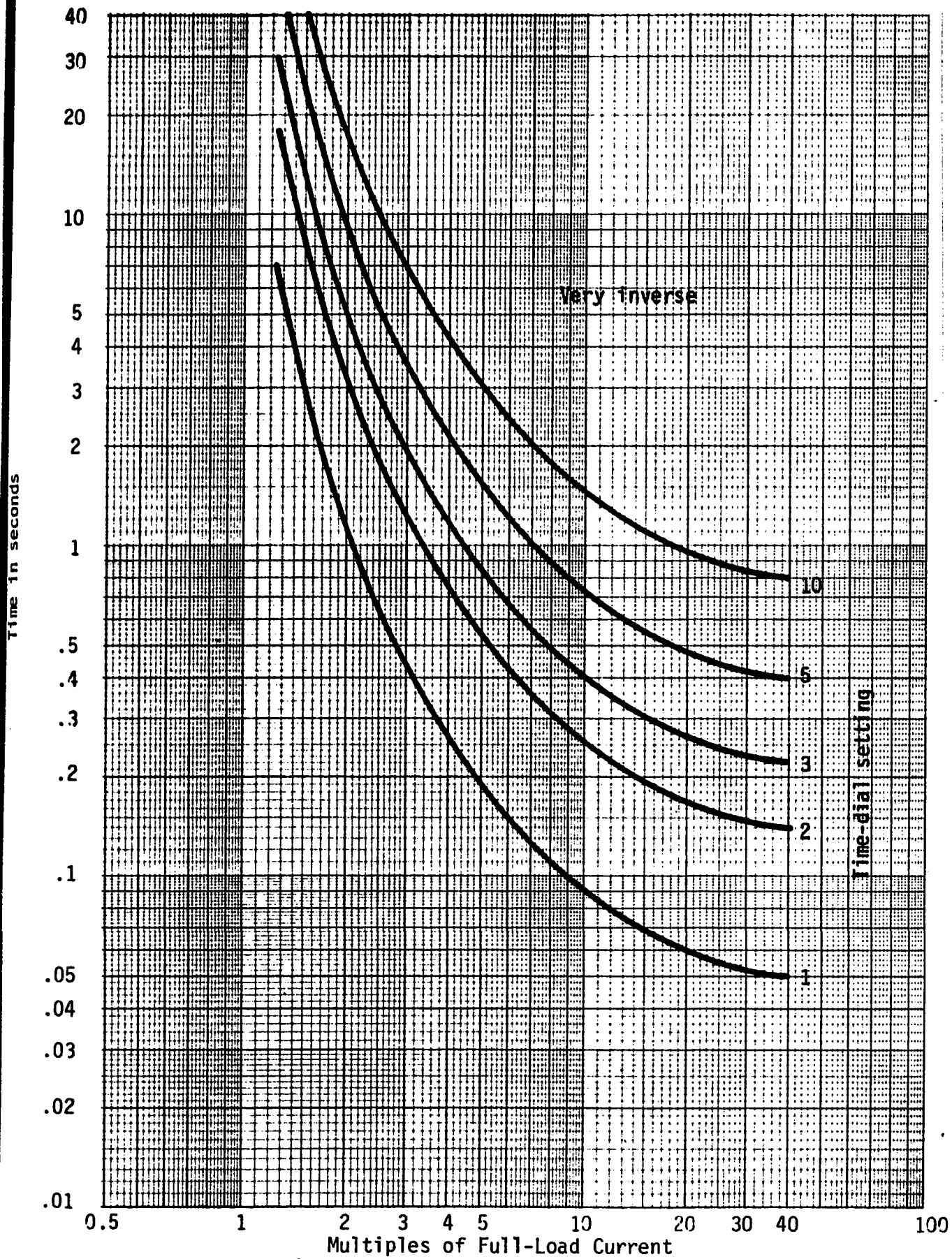


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

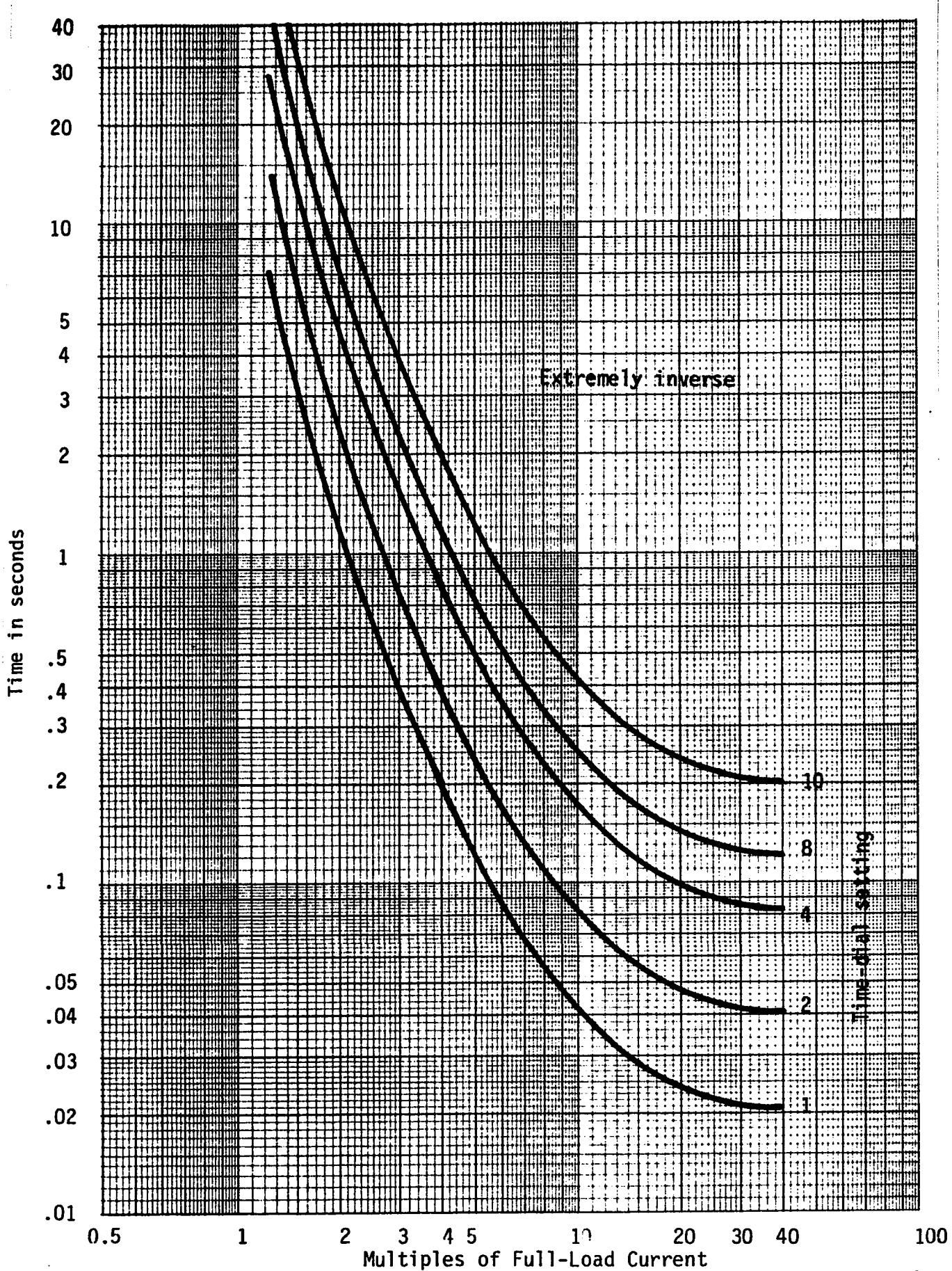


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

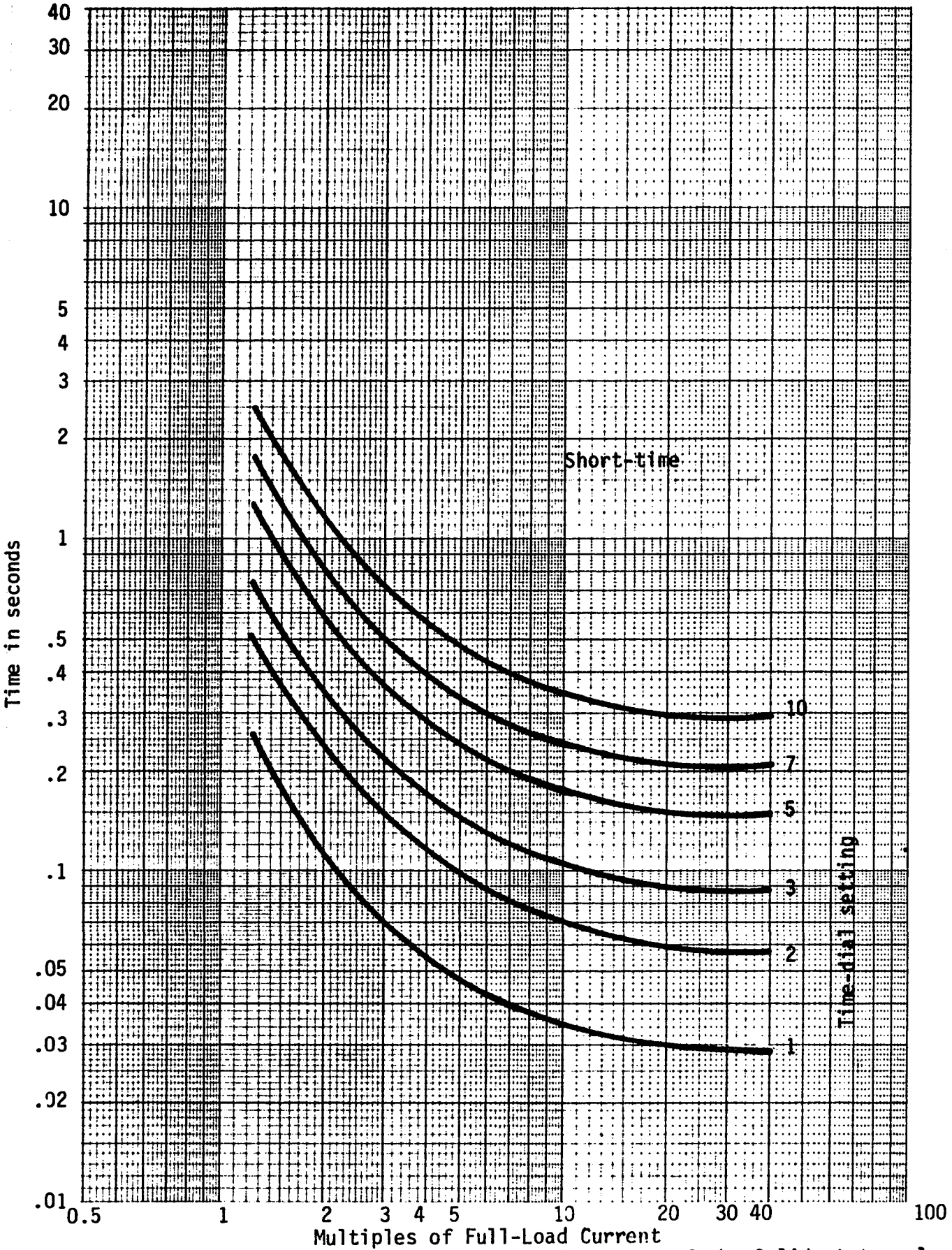


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

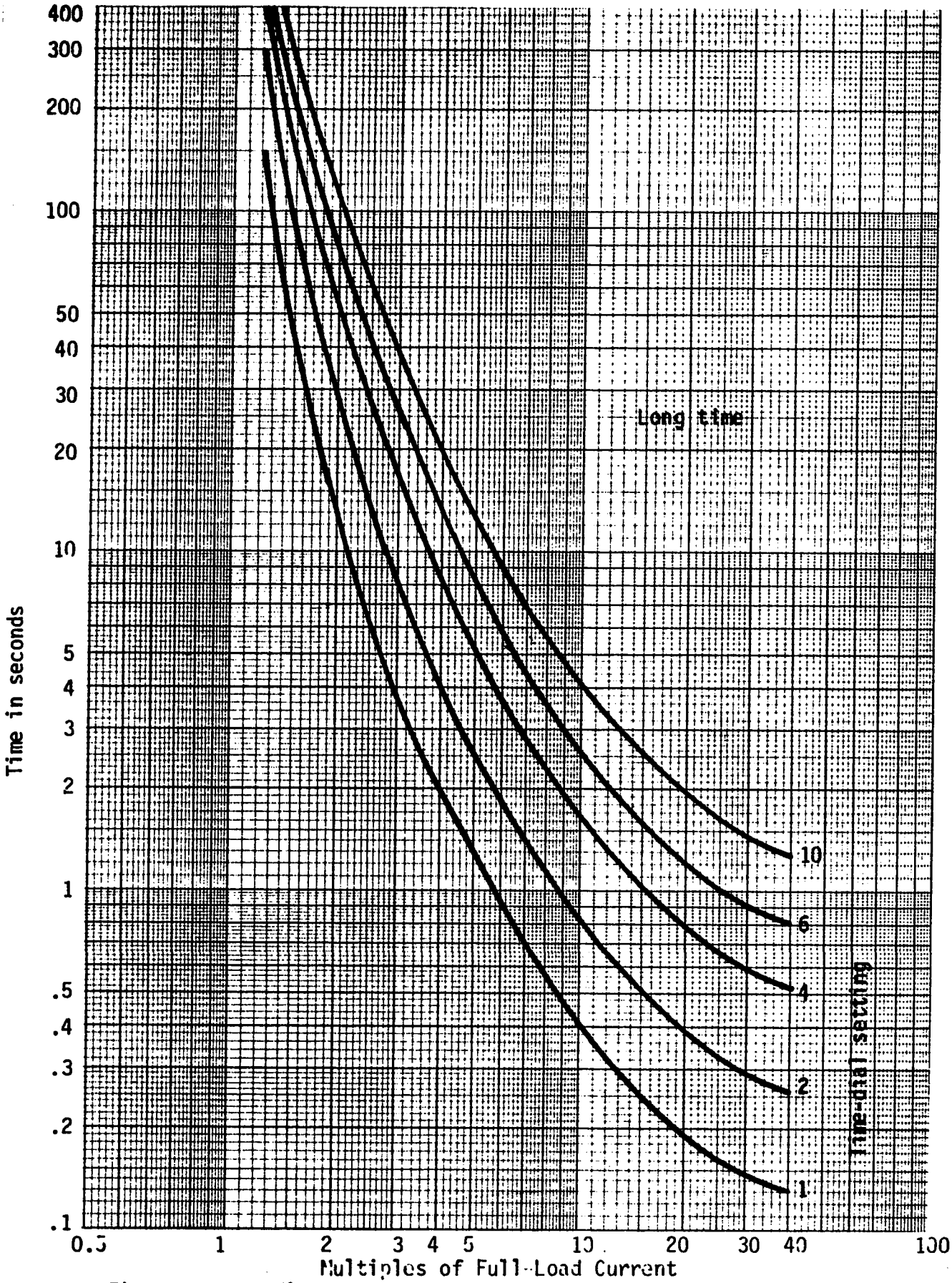


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

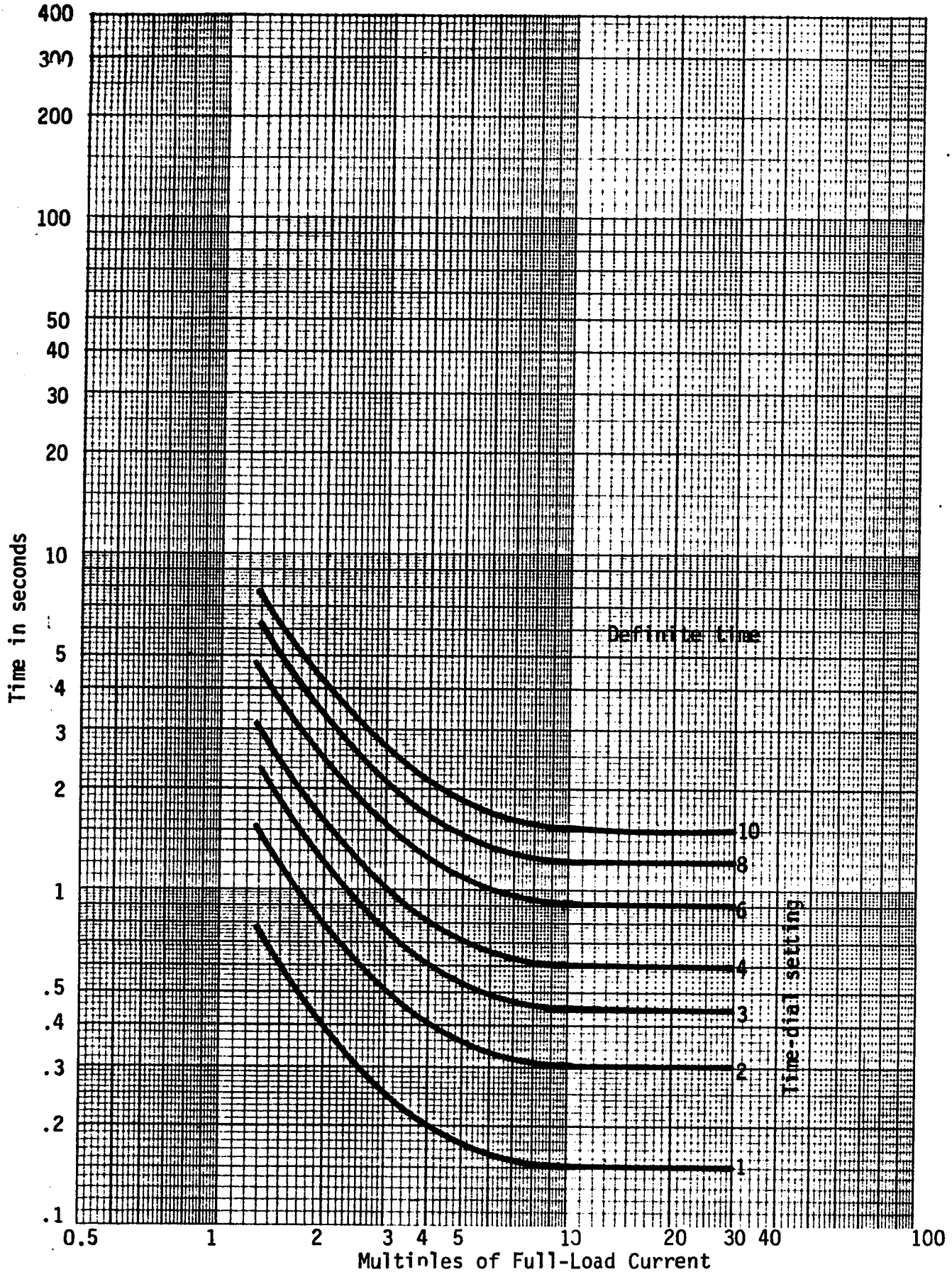


Figure 4.13. Time-Current Characteristic curves of the Solid-state relay.

Low burden is an important consideration in the application of all relays. Space and money savings result from low volt-ampere requirements from instrument transformers. Current transformer saturation effects can seriously deteriorate relay performance |13|.

The burden which a relay imposes on its current transformer is expressed in terms of the impedance (ohm) of its coil, or the product (volt-amperes), of the impedance times the current through the relay. Naturally, more turns are required in a coil to produce the necessary ampere-turns (torque) to operate a relay on low current than on high current. More turns in the coil mean higher impedance. It is desirable to keep the burden as low as possible, because the higher the burden the greater the possibility of current-transformer ratio breakdown due to saturation. The potential coils of relay also impose a volt-ampere burden on their potential transformers. The total burden must not exceed the rating of the potential transformers |35|.

The low burden requirements of digital overcurrent relays shows this improvement which is illustrated in Table X.

The digital overcurrent relay curves are sharper and narrower than the electromagnetic tripping device. This is due primarily to the characteristics of the digital device which can be set with much more precision than the electromagnetic device in relation to time for a given value of current.

TABLE X. Burden Comparison.

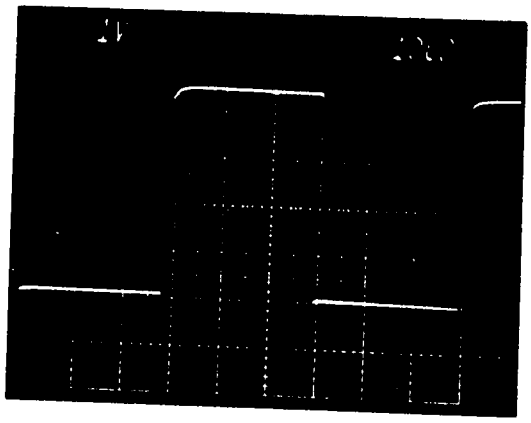
Relay Type	Burden in VA at 40 Amps.		
	Electromechanical	Solid-state	Digital
Extremely inverse	118	1.4	0.0205
Inverse	186	1.4	0.0205
Short-time	308	1.4	0.0205

Table XI shows a comparison based on the characteristics of each type of the relays in the three relay structures, electromagnetic, solid state and digital relays.

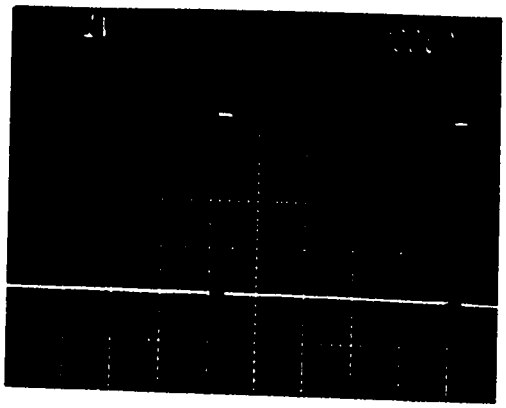
Figure 4.14 shows the outputs of a frequency divider. A 16 KHZ frequency was divided by 16 to get a 1 KHZ frequency and the latter was divided again by 4 to get another counting frequency of 250 HZ.

TABLE XI. Performance Comparison.

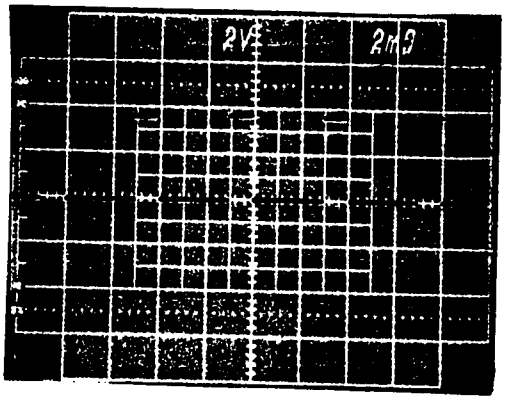
Relay structure / Relay type	Minimum Time in seconds that can be reached		
	Electromagnetic	Solid-state	Digital
Inverse time	0.14 - 0.6	0.12 - 1.2	<0.014 - 0.14
Very inverse time	0.072-1.4	0.06 - 8	<0.01 - 1.6
Extremely inverse time	0.025-1.6	0.02 - 8	<0.01 - 3.6
Short time	0.03 - 0.08	0.03 - 0.28	<0.015-0.16
Long-time	0.45 - 8	0.015 - 15	<0.013-16
Definite-time	-	0.15 - 0.8	<0.015-0.08



16 KHZ



1 KHZ



250 HZ

Figure 4.14. Frequency division photocopies.

5. MODIFICATION CIRCUITS

One of the most important advantages of this newly designed relay is that modifications can be introduced at any stage of the design or application. This makes this relay more applicable besides its simplicity. The same principle of operation can be used easily to serve other types and applications in the power system protection.

Impedance relaying, Differential relaying, as well as reverse power relaying will be explained and designed here as examples of these modification circuits.

5.1 DIGITAL IMPEDANCE RELAY

Impedance protection is a form which measures the distance between a relaying point and a fault and dependent on that measurement, the relay will be operative or inoperative. Since impedance is an electrical measure of distance along a feeder between two points, i.e. the ratio V/I, the relay can be designed to compare these impedance values, to recognize faults occuring within the protected section of the line from the fact that the distance from the relay to the fault is less than the setting of the relay [36].

It is known that the impedance of the transmission line cannot be calculated directly from the instantaneous values of

voltage and current but from their average values. In other words the impedance is given by equation 5.1

$$|Z| = \frac{V_p}{I_p} \qquad (5.1)$$

Thus an additional voltage signal can lead to an impedance relay by using a division procedure.

V_p and I_p can be obtained using the same technique of the digital over-current relay. The transmission line, to be protected, is usually divided into sections of certain lengths each has a defined well known impedance. Figure 5.1 shows the simplest system consisting of feeders in series, such that the power can flow only from left to right. If a short circuit occurs at point L between circuit breakers C and D, the impedances at A, B, C are $Z_A + Z_B + Z$, $Z_B + Z$, and Z respectively. The relays are set to operate with impedances less than Z_A, Z_B, and Z_C respectively,so that only relay C will operate $|27|$.

Thus dividing V_P by I_P at point C will give the value of the impedance $|Z| = \frac{V_P}{I_P}$. This value will be compared continuously with Z_C. Usually when a fault happens Z is less than Z_C. The block diagram describing this principle is shown in Fig. 5.2.

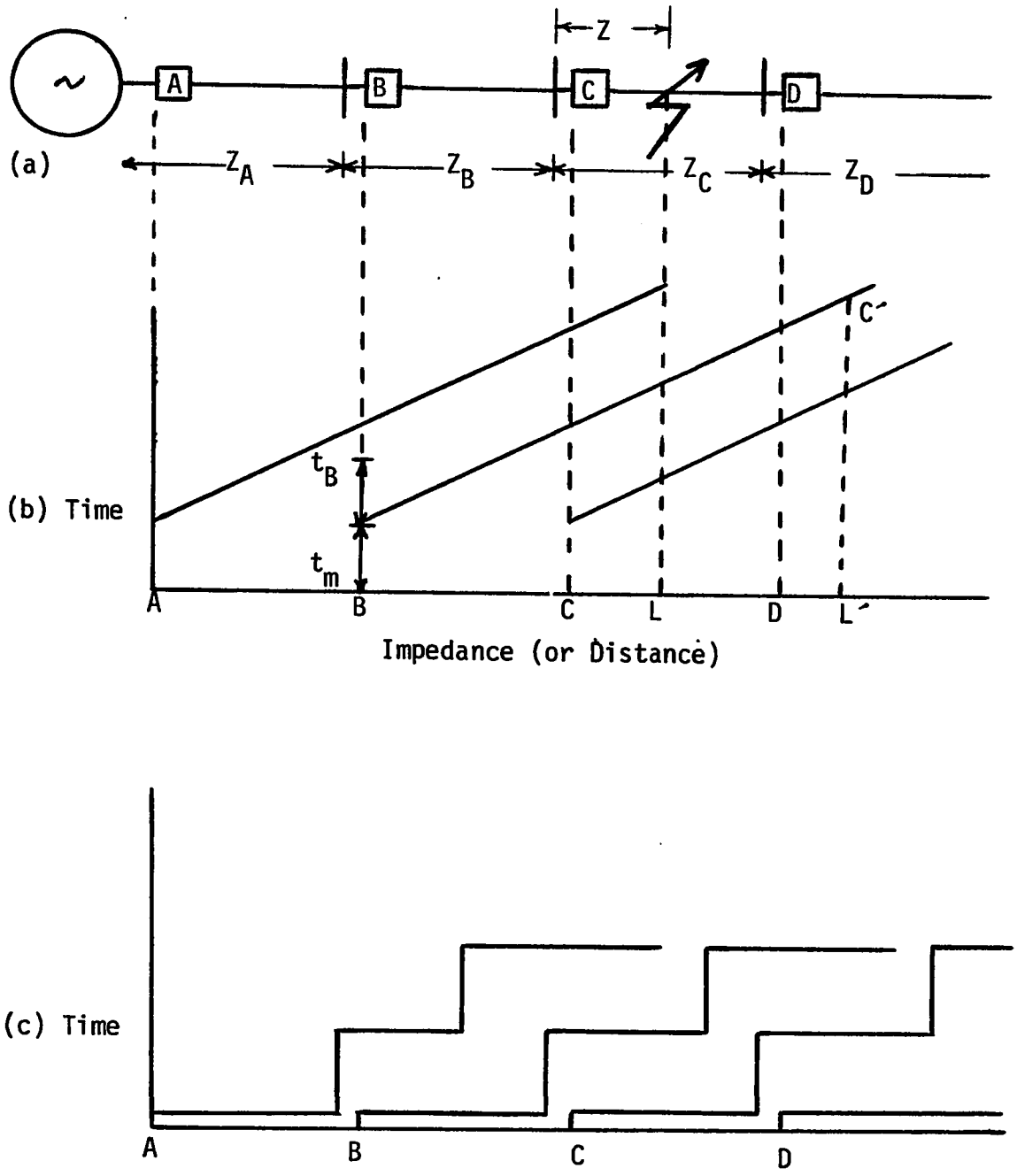


Figure 5.1. Distance or Impedance Protection.

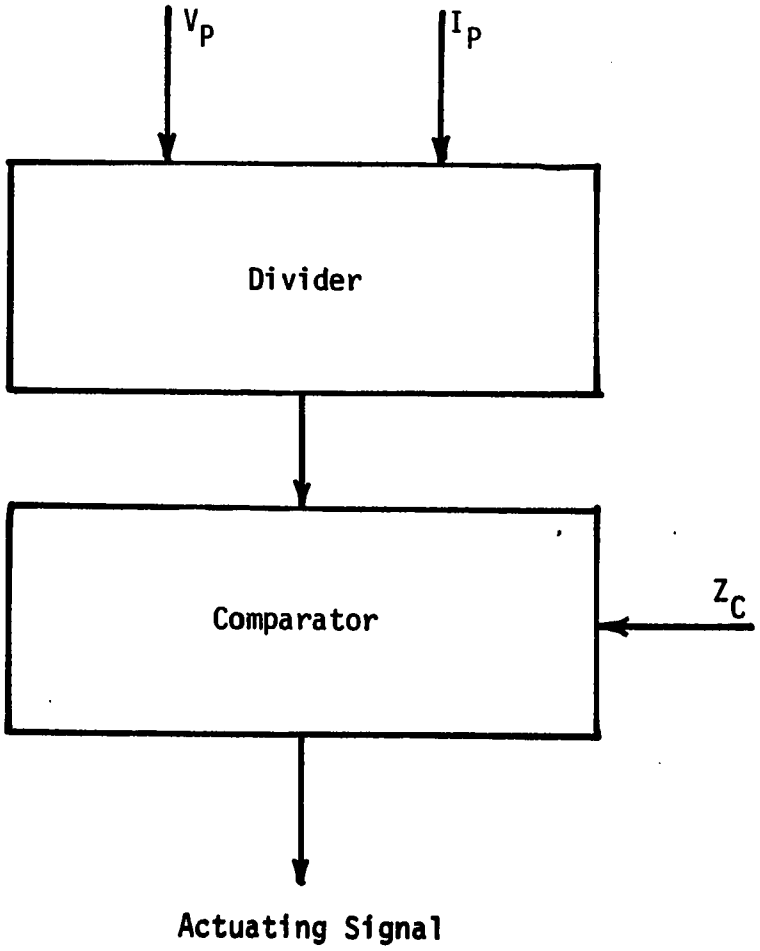


Figure 5.2. Principle of impedance relaying.

The Digital impedance relay consists of the following sections as shown in Fig. 5.3:

i) Section I for the determination of V_p.

ii) Section II for the determination of I_p.

iii) Section III for the sequence controller.

iv) Section IV for the calculation and comparison of the impedance for the defined section of the transmission line.

Sections I and II are identical to the sampling and error formulation sections of the digital over current relay.

In Section III an additional control signal C3 is added to start the division process at the right time. The purpose of this control signal, C3, is to allow enough time for the loading of data in registers R_{V_p} and R_{I_p}. Control signals C1 and C2 are given at the same time to both sections I and II to make sure that the relative values of V_p and I_p are divided by each other.

In Section IV the calculated impedance Z is compared with the original impedance of that certain section to be protected. If $Z < Z_c$, then a tripping signal should occur to open the respective circuit breaker to isolate the faulty section.

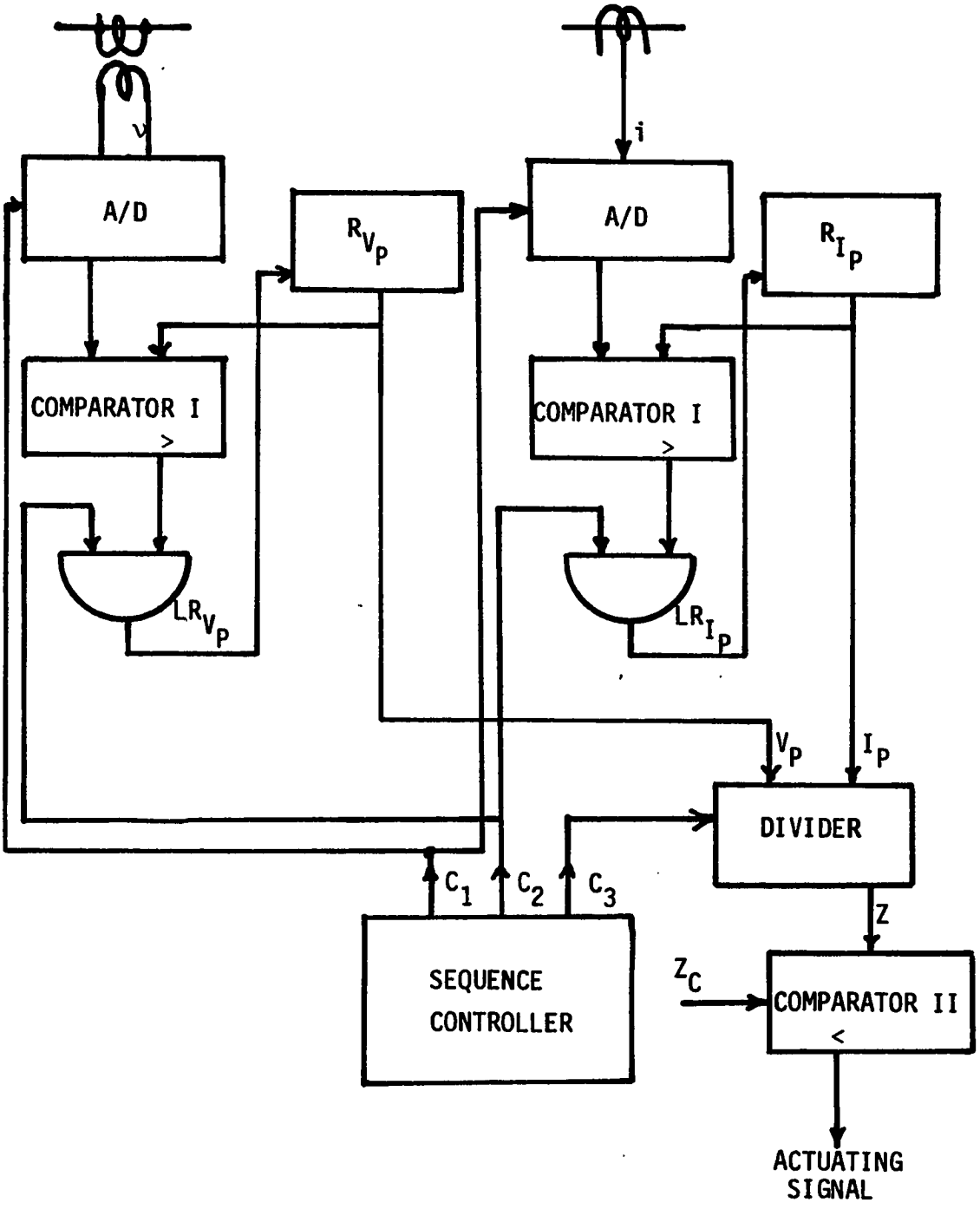


Figure 5.3. Block diagram of the digital impedance relay.

The state diagram for the digital impedance relay is shown in Fig. 5.4.

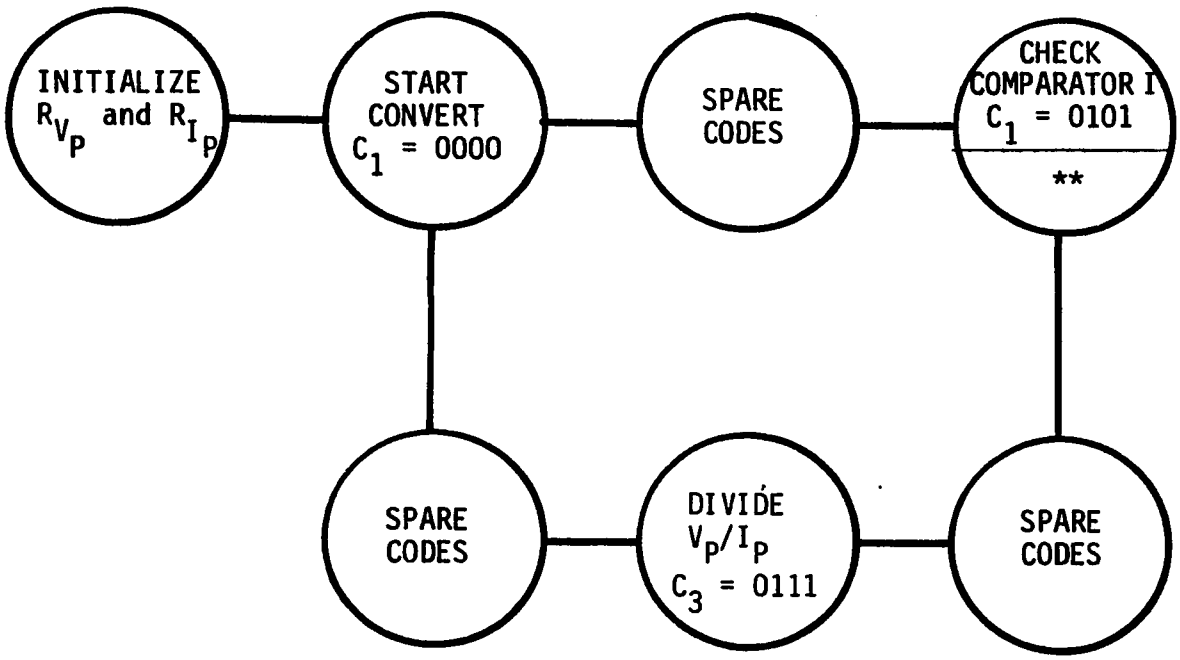
The sequence controller consists of the master clock and a binary counter as its commutator circuit, as shown in Fig. 5.5(a). The control signals logic circuit is shown in Fig. 5.5(b), where A, B, C, and D are the outputs of the binary counter and A is the LSB and D is the MSB.

The master clock frequency is identical to that of the digital overcurrent relay and is equal to 16 KHZ.

5.2 DIFFERENTIAL PROTECTION

Figure 5.6 shows the basic differential connection. Faults inside the machine generally develop as a ground in one of the phase windings and often spread to involve more than one phase. By far the most effective protection of such faults is the differential protection. In this scheme, the currents in each phase on either side of the machine are compared in a differential circuit and any unbalance or difference current is used to operate a relay. For normal operation or for a fault outside the two sets of current transformers, I_1 entering the machine equals I_2 leaving the machine in all phases (neglecting the small internal losses) and assuming perfect transformers.

The relay current, $I_1 - I_2$, then is small, and the relay can be set above its maximum value during normal machine operation



** IF ">" is high LR_{V_P} and/or LR_{I_P}

Figure 5.4. State diagram for the digital impedance relay.

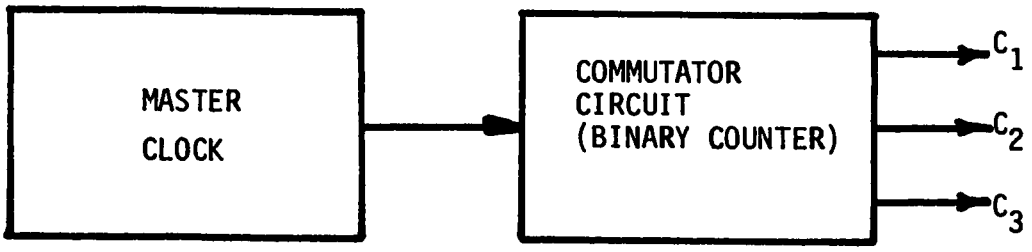


Figure 5.5(a). Sequence Controller.

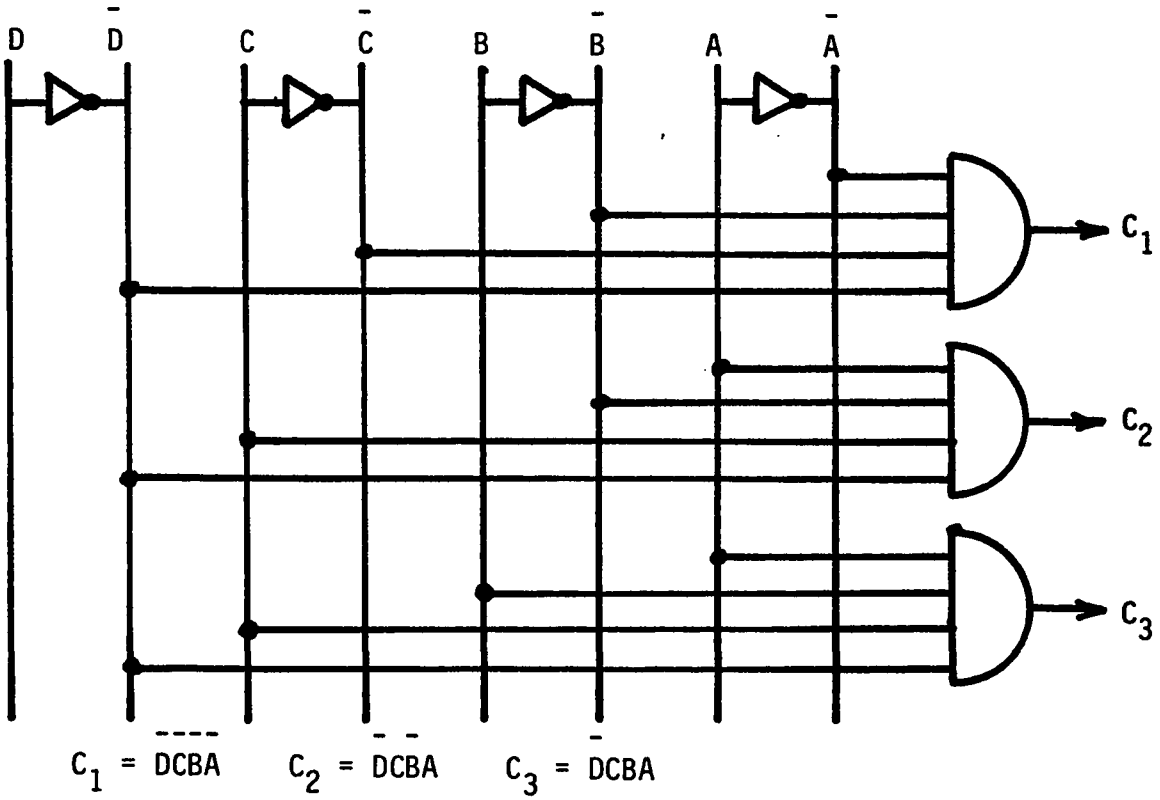


Figure 5.5(b). Control signals logic circuit.

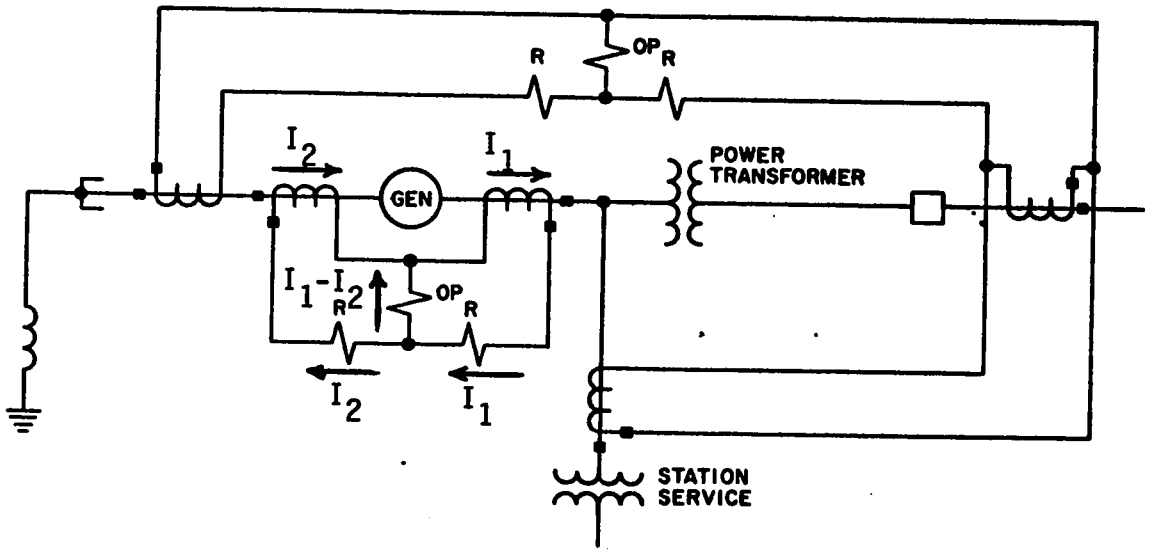


Figure 5.6. The basic differential connection.

to prevent relay operation. When a fault occurs between the two sets of current transformers, one or more of the currents I_1 suddenly increases, while the current I_2 may decrease or suddenly increase and flow in the reverse direction. In any event, the fault current now flows through the relay to operate it |37|. Figure 5.7 shows the block diagram of the digital differential relay.

The digital differential relay consists of two current transformers connected on either side of the machine or sides of transformer or certain length of transmission line. Two A/D converters are used to convert the current samples into binary values. These binary values of current I_1 and I_2 are stored in registers R_{I_1} and R_{I_2} respectively. The contents of R_{I_1} and R_{I_2} are subtracted using a binary adder. The resulting error signal is then compared with a preset value to decide on fault/no fault situation. If the error signal is greater than the preset value, then a fault has happened and a tripping signal should be initiated.

Two control signals C1 and C2 are used in this scheme. C1 is fed to both A/D converters to start the conversion process while C2 is fed to both registers R_{I_1} and R_{I_2} as a loading signal with the new binary values of the successive samples.

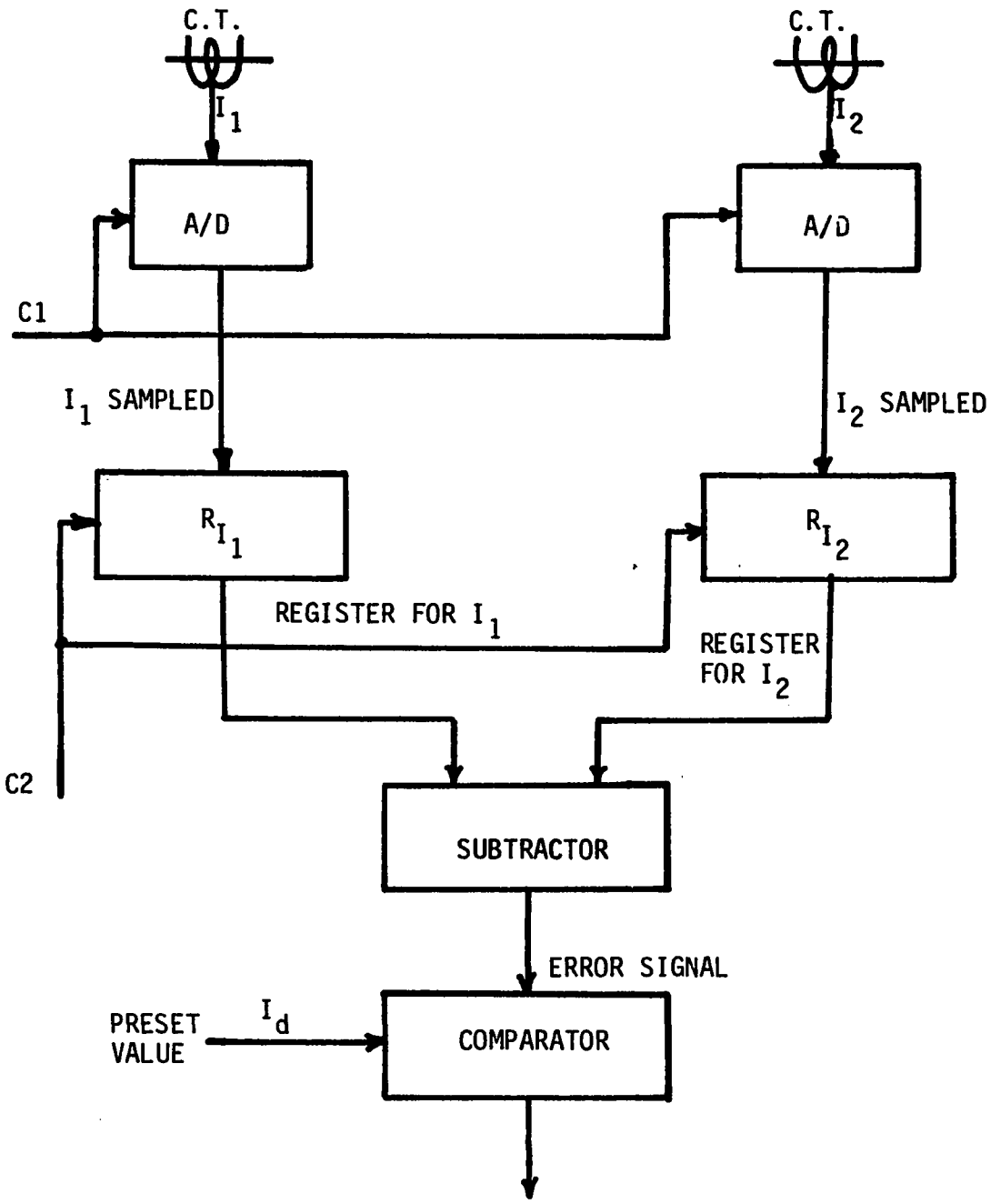


Figure 5.7. Block diagram of the digital differential relay.

Figure 5.8 shows the state diagram of the digital differential protection relay. The sequence Controller for the differential protection consists of a master clock, whose frequency is 16 KHZ to be used, and a 4-bit binary counter to represent the commutator circuit. This is shown in Fig. 5.9.

If the outputs of the binary counter are D, C, B, and A where A is the LSB and D is the MSB, then the control signals C1 and C2 are given by,

$$C1 = \bar{D}\,\bar{C}\,\bar{B}\,\bar{A}$$

and $$C2 = \bar{D}\,C\,\bar{B}\,A \quad ,$$

which means that C1 will start at zero time and C2 will be after 312.5 μ sec which is enough for the A/D conversion process to complete the A/D converter needs 200 μ sec to reach its full scale value.

5.3 DIGITAL REVERSE POWER RELAY

The reverse power relay can be classified under the directional relays in which the direction of the power flow is important. The normal direction of the power flow will cause no relay operation. A reverse of power happens in a generator for example when the input power to the prime mover is cut-off. In this case the generator will be fed from another generator in the

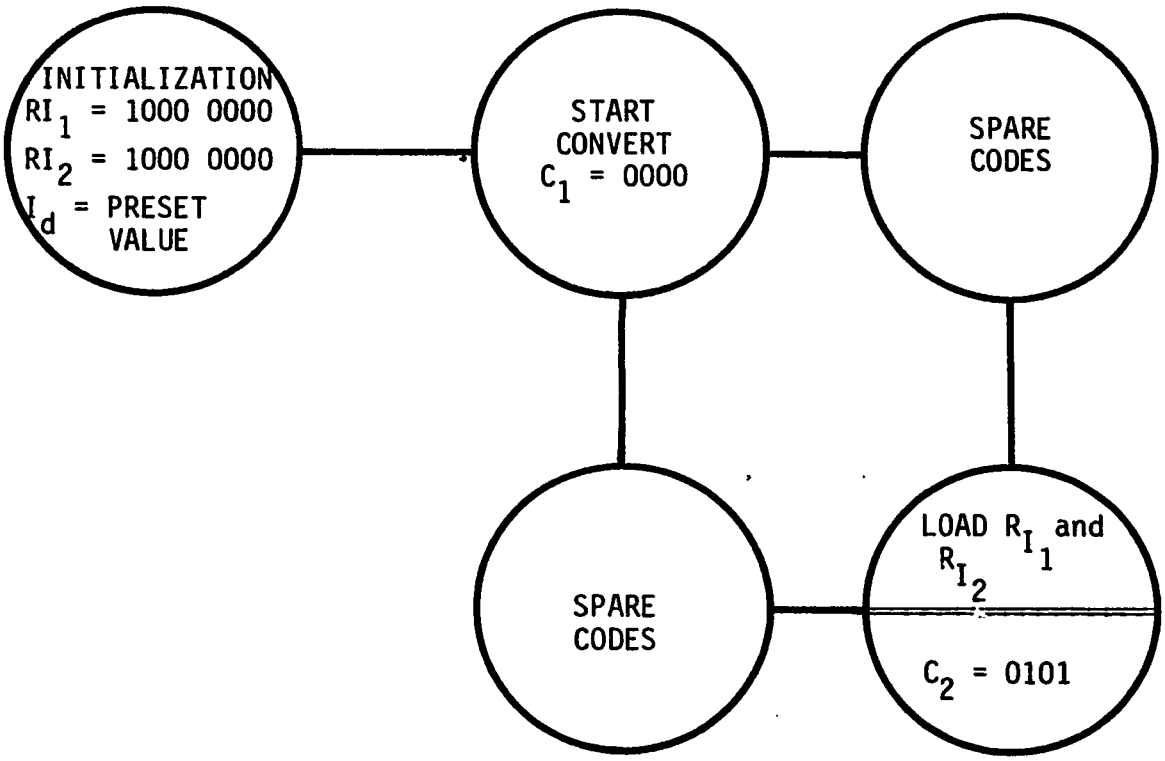


Figure 5.8. State diagram of the digital differential protection relay.

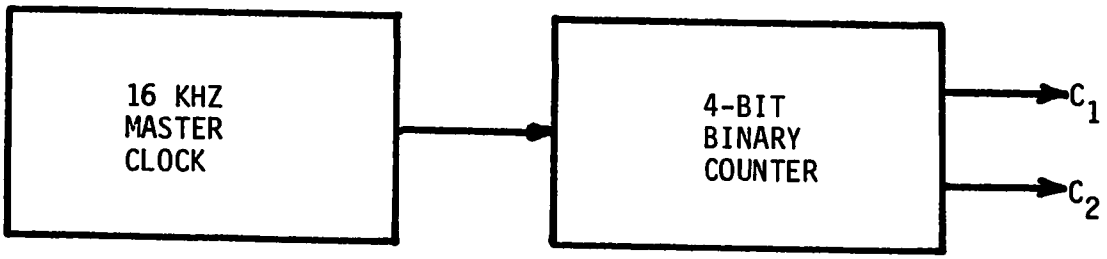
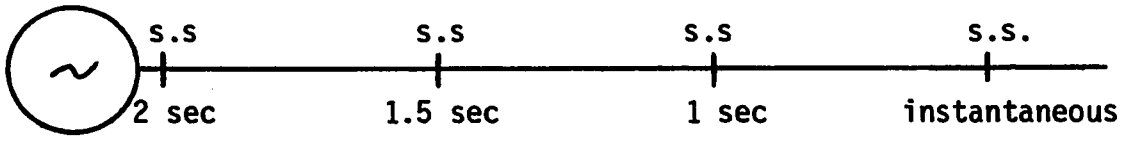


Figure 5.9. Sequence Controller.

power system and will act as a motor. The instance this failure happens, the reverse power relay should sense it and order the appropriate circuit breaker to open and disconnect that particular generator. Another application of these relays is in the protection of lines and cables. It is, of course, highly undesirable that all the overload relays in a system should operate as soon as a fault occurs, for then the whole system is shut down. In radial system the smallest possible part of the system is switched out by having relays with an inverse time characteristic with a definite minimum. The minimum time is arranged in or decreasing order as the distance from the generator increases. The same principle applies, of course, to a number of feeders in series as shown in Fig. 5.10, but not to feeders in parallel, as shown in Fig. 5.11. Parallel feeders may be protected by overload (A and B) and reverse power relays (C and D) as shown in Fig. 5.11. If a fault happens at X, power flows around AC DX and relay D operates. Then B will operate and the faulty feeder is cutout |27|.

5.4 PROTECTION AGAINST MOTORING OF A GENERATOR

The application of motoring protection utilizing electrical quantities is recommended on all machines. This type of protection is provided by limit switches, exhaust hood temperature detector, etc., but where a large number of these devices are involved, the



s.s. substation

Figure 5.10. Number of feeders in series.

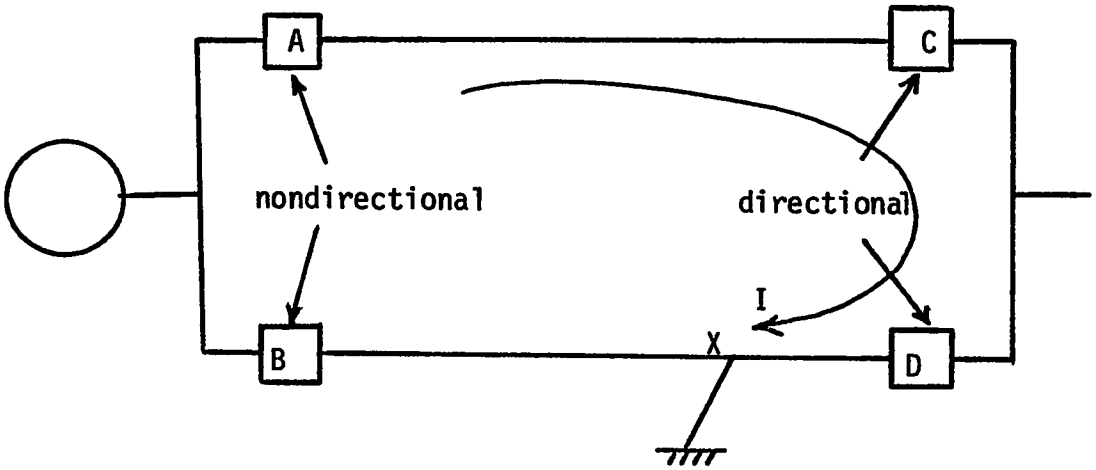


Figure 5.11. Number of feeders in parallel.

simplicity of a single reverse power protective relay is attractive in providing added safety and back-up protection.

Motoring occurs as a result of a deficiency in the prime mover input to the a-c generator. As a result, the real power will be fed to the machine. This can be detected by comparing the power generated by the generator with that before the bus. Instantaneous samples of ν and i are multiplied and accumulated over a period of half a cycle. Then this accumulated power is divided by the number of samples taken within that period.

A zero crossing detector can be used to determine the start and the end of the calculating period $(\frac{T}{2})$.

The power supply frequency is 60 HZ, or T = 16.6667 m sec, which means 32 samples per cycle are taken, then sampling time is $T_s = \frac{16.6667}{32}$ m sec., and the sampling frequency is f_s = 1920 HZ. The average power is calculated by:

$$P_{av.} = \frac{\nu_1 i_1 + \nu_2 i_2 + \nu_3 i_3 + \text{---} + \nu_{16} i_{16}}{16} \qquad (5.2)$$

The sampling and data transfer takes place when the value of the signal is not zero. This is controlled by the zero detector, which gives "1" when the value is not zero. This is ANDed with the sampling frequency f_s using the AND gate A_1 shown in the designed circuit given in Fig. 5.12. At the same time no data is allowed to

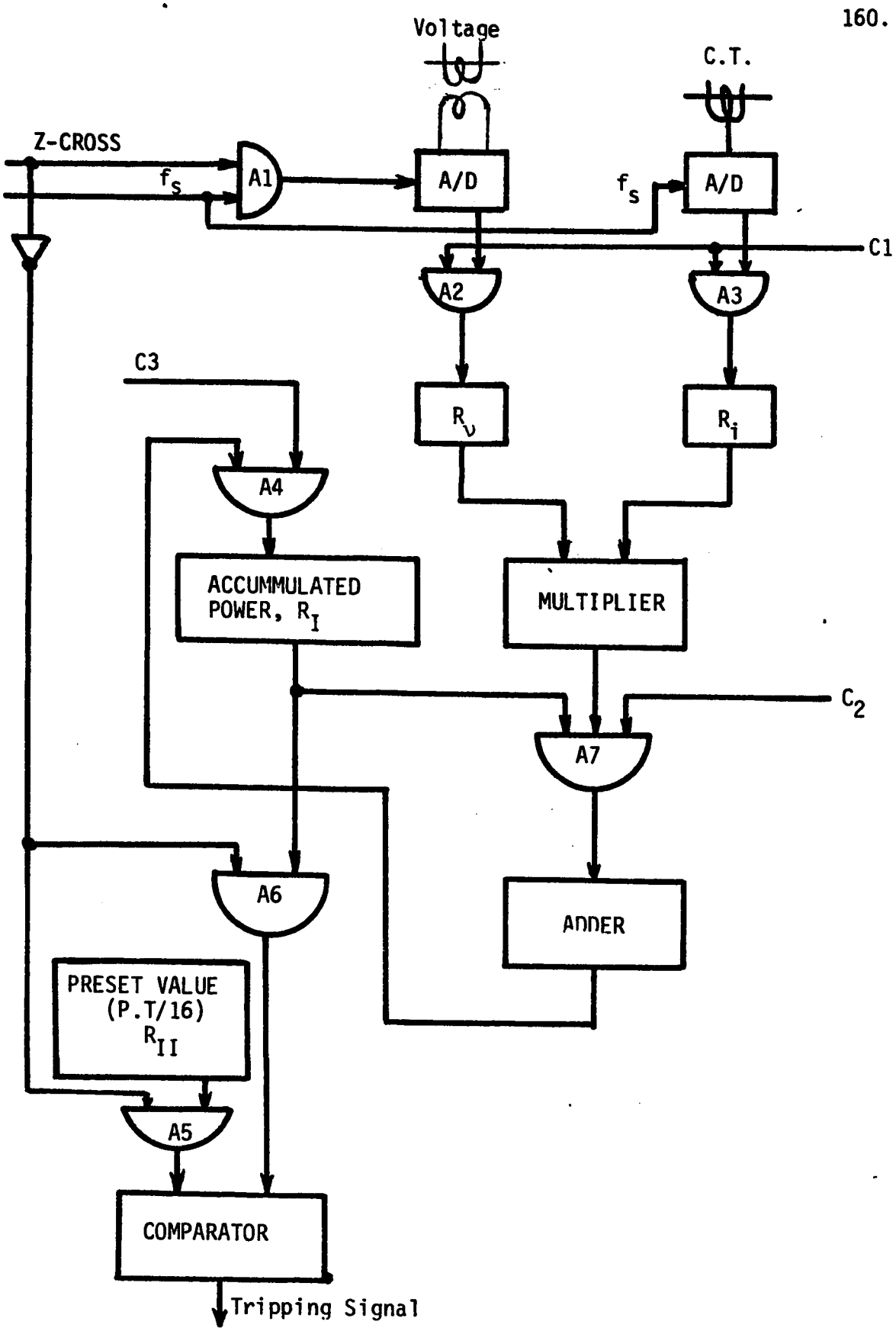


Figure 5.12. Digital Reverse Power Relay.

enter the inputs of the comparator. On the other hand, when a zero value is detected, we will have "1" at the output of the inverter gate, which is ANDed with both data of registers R_I and R_{II} thus allowing these data to appear at the inputs of the comparator.

Control signals C1, C2, and C3, are used to control the operation of this relay.

The control signal C1 is used to load the registers R_v and R_i with the voltage and current samples respectively. It should be identical to the sampling frequency, except that it should be delayed by more than 200 μ sec after the zero detection to make sure that the conversion process has been completed. This is performed by the two AND gates A_2 and A_3.

The control signal C2 is used to control the addition operation. It allows the accumulated power data of register R_I and the new product sampled power to appear at the inputs of the adder at the right time thus giving enough time for the multiplication process to be completed. The control signal C3 is used to load the register R_I with the resultant accumulated power after the addition process has been completed. C2 and C3 are also identical to the sampling frequency.

Figure 5.13 shows the state diagram of the reverse power relay.

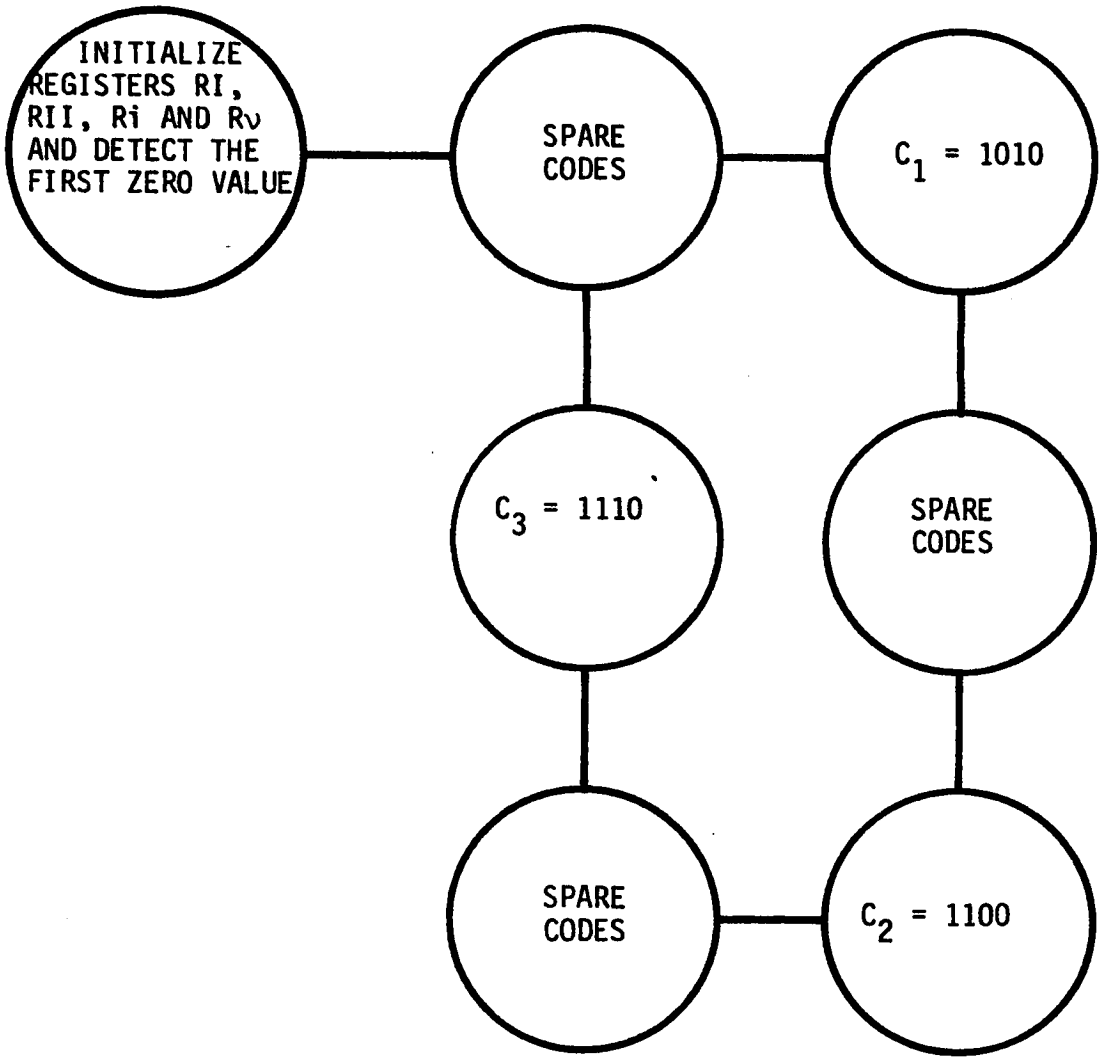


Figure 5.13. State diagram.

Figure 5.14 shows the sequence controller block diagram and the logic circuit for the control signals C_1, C_2, and C_3.

The design of these modification circuits can be altered depending on the application it is used for and also the current and voltage signals can be forwarded to any type of these relays by the addition of a multiplexer.

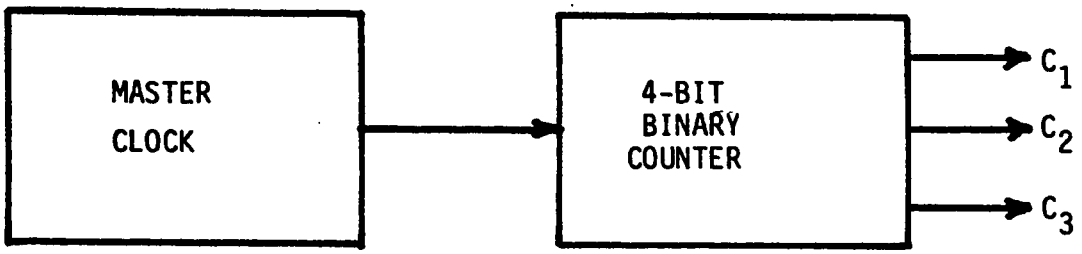


Figure 5.14(a). Sequence Controller.

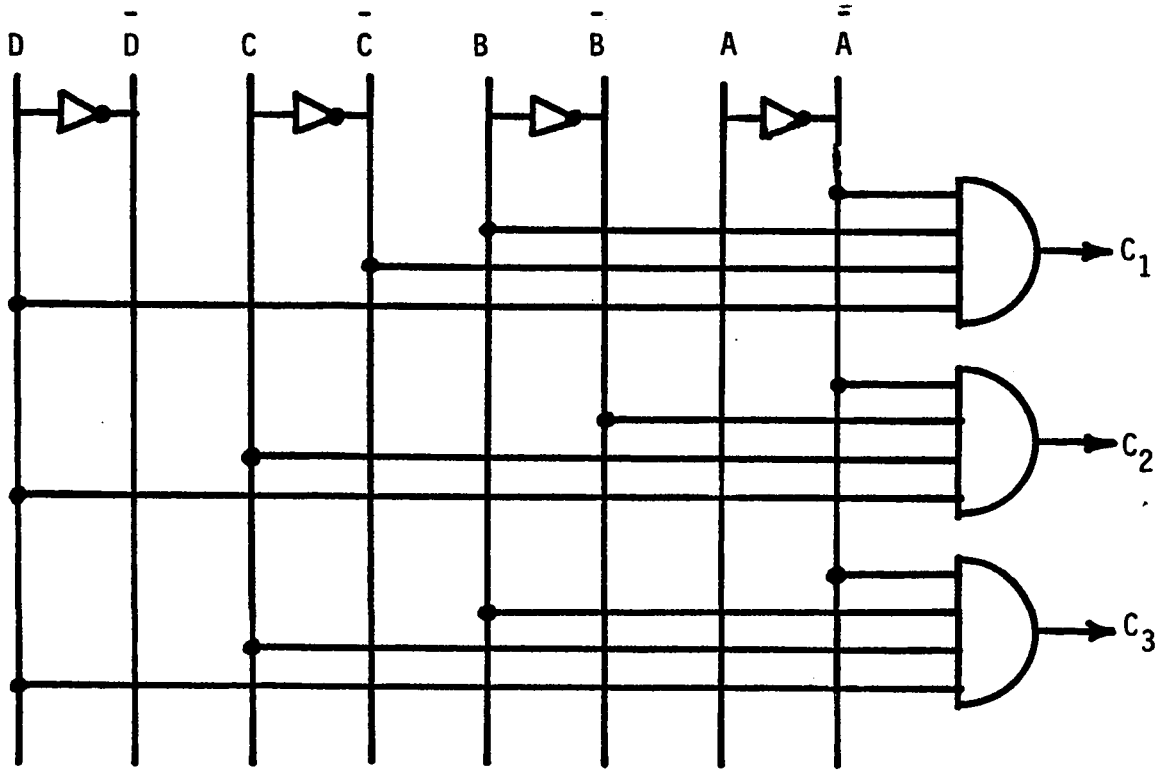


Figure 5.14(b). Logic Circuit.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The test results obtained from this prototype digital overcurrent relay clearly demonstrate the feasibility of such a unit for power system protection. A single over-current relay unit can protect all types of devices by only modifying the settings of the preset values of the Registers. Different Time-Current Characteristic curves could be obtained by changing the counting clock frequency, CK2, used to trigger the Delay Counters. There is no effect of mechanical inertia and friction. The shapes of the characteristic curves are changed by changing the strappings of the outputs of the delay counters. The characteristic curves could be smoothen out by adding more registers and comparators in the actuating controller circuit. The modification circuits, which can be added at any stage of the design or application, allows the operator to use this single unit for more than one purpose at the same time.

On-line computer control can be used for assigning the preset values and getting also the output control signals. These types of digital relays can be designed with the same input output ratings as the electromagnetic relays while eliminating the problems associated with the moving parts.

This newly designed relay is more selective, sensitive, and reliable than the existing ones. It performs its

function adequately for the period of time intended under the operating conditions with a high probability of success. Comparison of results with solid-state and electromagnetic relays shows that this relay has many advantages in applications and more wide varied time current characteristics. They have sharper and narrower curves besides the lower tripping time which allows for small-difference in coordination applications.

This relay is able, within 1 m sec, to decide on fault/no fault situations or even less than this time by choosing a higher sampling frequency.

Thus the variety of relay characteristics and the ease and flexibility of protective applications are some of the more attractive features of these digital relays.

Other benefits include information supplied to the trip report. The time of the fault, the fault duration, the operating time of the relaying system the fault type, the approximate location of the fault. These information are usually obtained in the conventional relays by using an automatic oscillograph and event recorders. While in digital systems, this could be obtained by using an on-line computer connected to these protective devices which would give instant display or printed message.

Further research on the hardware digital overcurrent relay should concentrate on improving the quality of signals, and setting

points using the station on-line computers. Use of the modified relays based on the scheme outlined in this thesis could lead to a complete hardware digital protection system.

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APPENDIX A

I) The analog to digital converter (ADC-89A):

It is manufactured by Data Systems, Inc. The following tables show the input/output connections of the A/D converter, and the output coding respectively. A figure showing the conversion time is also present.

TABLE XII. INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1.	E.O.C. (STATUS)
2.	BIPOLAR OFFSET
3.	START CONVERT
4.	CLOCK OUT
5.	BIT 1 OUT (MSB)
6.	BIT 2 OUT
7.	BIT 3 OUT
8.	BIT 4 OUT
9.	BIT 5 OUT
10.	BIT 6 OUT
11.	BIT 7 OUT
12.	BIT 8 OUT (LSB)
17.	+ 5V POWER IN
18.	+ 15V POWER IN
19.	- 15V POWER IN
20.	POWER GROUND
31.	ANALOG GROUND
32.	ANALOG IN

TABLE XIII. BIPOLAR (-5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY
+FS-1 LSB	+ 4.96V	1111 1111
+3/4 FS	+ 3.75V	1110 0000
+1/2 FS	+ 2.50V	1100 0000
0	0.00V	1000 0000
-1/2 FS	-2.50V	0100 0000
-3/4 FS	- 3.75V	0010 0000
-FS+1 LSB	- 96.V	0000 0001
-FS	- 5.00V	0000 0000

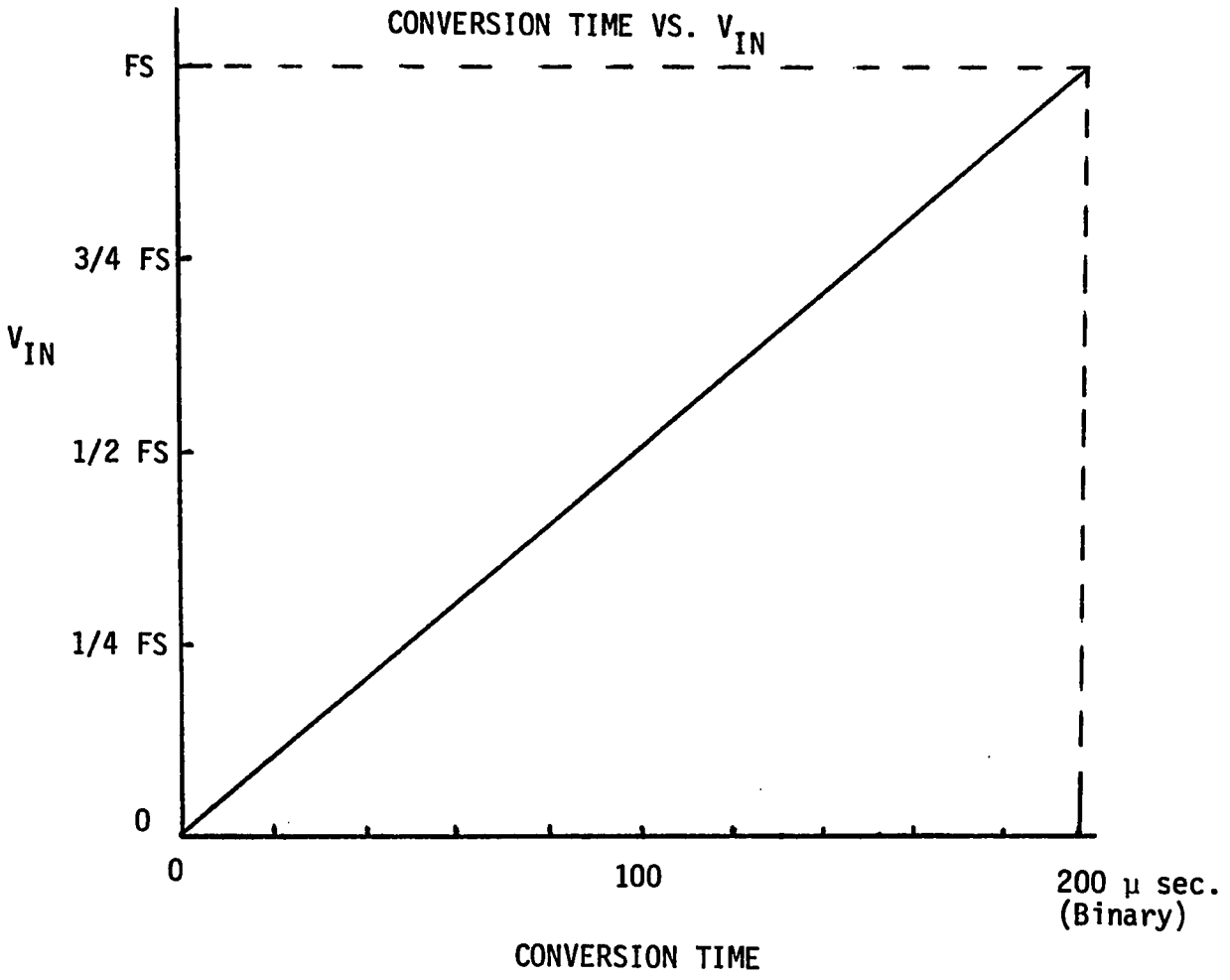

Figure A.1. Conversion time against input voltage.

Some specifications of the A/D converter used:

Analog input range	:	$\pm$ 5V F.S.
Start conversion	:	2V min. to 5.5V max. Positive pulse with duration of 150 n sec min. Logic "1" resets conversion Logic "0" initiates conversion.
Parallel output Data	:	8 parallel lines of data held until next conversion command. Vout ("0") $\leq$ + 0.8V Vout ("1") $\geq$ + 2.4V
Coding, Bipolar operation	:	Offset binary, positive true
End of conversion (EOC):		Conversion status signal Vout("0") $\leq$ + 0.8V indicates conversion completed. Vout ("1") $\geq$ + 2.4V during reset and conversion period.
Clock output	:	Internal clock pulse train of 320 n sec. 0 to + 5V pulses gated on during conversion time (255 = 2^8 - 1 FS binary)

Resolution	:	8 bits (1 part in 256) for binary.
Accuracy at $25^{o}C$	:	$\pm$ 0.2% of FS $\pm \frac{1}{2}$ LSB.

II) The digital to analog converter (DAC-9):

The following tables show the input output connections and the input coding of this converter respectively.

TABLE XIV. Pin Connections of DAC.

PIN	FUNCTION DAC-9-8B1
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8 (LSB)
9	+15V POWER INPUT
10	FULL SCALE TRIM (2)
11	COMMON GROUND
12	ANALOG OUTPUT
13	NOT USED
14	NOT USED
15	NOT USED
16	NOTE USED
17	NOT USED
18	NOT USED
19	NOT USED
20	NOT USED

TABLE XV. Input Coding for DAC 9 Series - Voltage Output Versions.

ANALOG OUTPUT RANGE (± 5V, FS)	BINARY (ONLY) 2'S COMPLEMENT
8 BITS	
+ 4.960	01111111
+ 4.375	01110000
+ 3.750	01100000
+ 2.500	01000000
0.000	00000000
- 2.500	11000000
- 3.750	10100000
- 4.375	10010000
- 5.000	10000000

APPENDIX B

DIGITAL COMPARATOR: It is sometimes necessary to know whether a binary number A is greater than, equal to, or less than another number B. The system for making this determination is called a magnitude digital (or binary) comparator. Consider single bit numbers first. The exclusive NOR is an equality detector because:

$$E = \overline{A\bar{B} + \bar{A}B} = \begin{matrix} 1 \\ 0 \end{matrix} \begin{cases} A = B \\ A \neq B \end{cases}$$

The condition A > B is given by:

$$C = A\bar{B}$$

because if A > B, then A = 1 and B = 0, so that C = 1. On the other hand, if A = B or A < B (A = 0, B = 1), then C = 0 Similarly the restriction A < B is determined from:

$$D = \bar{A}B$$

The logic block diagram for the nth bit drawn in the following figure has all three desired outputs C_n, D_n, and E_n. It consists of two inverters, two AND gates and the AOI (AND-OR-INVERT) circuit.

Alternatively, this figure may be considered to consist of an EXCLUSIVE-NOR and two AND gates.

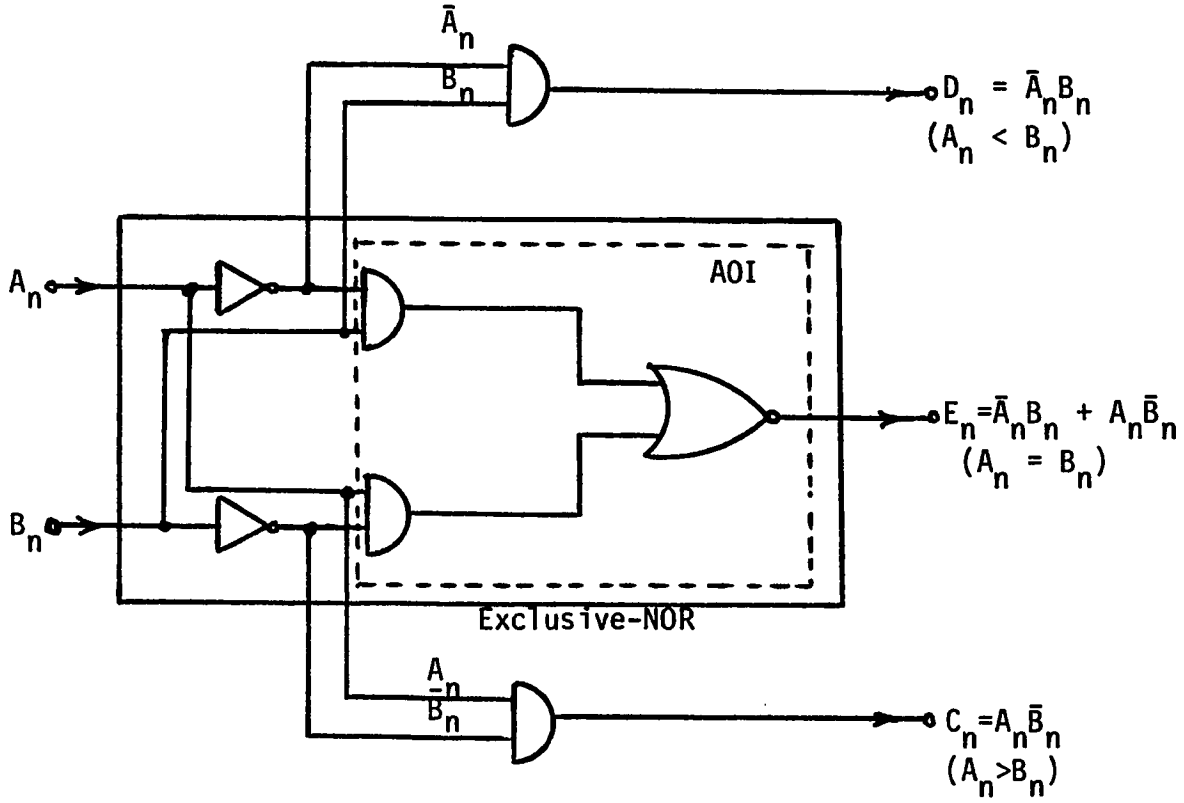

Figure B.1. A 1-bit digital comparator.

. Consider now a 4-bit comparator.

A = B requires that :

$$A_3 = B_3 \text{ and } A_2 = B_2 \text{ and } A_1 = B_1 \text{ and } A_0 = B_0.$$

Hence the AND gate E in Fig. 3.9 described by $E = E_3E_2E_1E_0$ implies A = B if E = 1 and A ≠ B if E = 0 (Assume that the input E´ is held high; E´=1)

The inequality A > B requires that

$$A_3 > B_3 \text{ (MSB)}$$

or

$$A_3 = B_3 \text{ and } A_2 > B_2$$

or

$$A_3 = B_3 \text{ and } A_2 = B_2 \text{ and } A_1 > B_1$$

or

$$A_3 = B_3 \text{ and } A_2 = B_2 \text{ and } A_1 = B_1 \text{ and } A_0 > B_0$$

The above conditions are specified by the Boolean expression.

$$C = A_3\bar{B}_3 + E_3A_2\bar{B}_2 + E_3E_2A_1\bar{B}_1 + E_3E_2E_1\,A_0\bar{B}_0$$

if and only if C = 1. The AND-OR gate for C is indicated in Fig. 3.9 (Assume that C´ = 0).

The condition that A < B is obtained from equation by interchanging A and B. Thus

$$D = A_3B_3 + E_3A_2B_2 + E_3E_2\bar{A}_1B_1 + E_3E_2E_1\bar{A}_0B_0$$

implies that A < B if and only if D = 1.

This portion of the system is obtained from Fig. 3.9 by changing A to B, B to A, and C to D. Alternatively, D may be obtained from $D = \bar{E}\bar{C}$ because, if $A \neq B$ ($E = 0$) and if $A \not> B$ ($C = 0$), then $A < B$ ($D = 1$).

The SN 7485 digital comparator has a typical compare time = 21 n sec. and typical power dissipation = 275 mw.

These devices are fully expandable to any no. of bits without external gates. Words of greater length may be compared by connecting comparators in cascade as follows:

1) The $A > B$, $A < B$, and $A = B$ outputs of a stage handling the LSB are connected to the corresponding $A > B$, $A < B$, & $A = B$ inputs of the next stage handling the MSB.

2) The stage handling the LSB must have a high-level voltage applied to its $A = B$ input.

APPENDIX C

4-Bit Shift Registers (SN 7495A):

These are parallel-in, parallel-out 4-bit registers.

Since a binary is a 1-bit memory, then n flip-flops can store an n-bit word. This combination is referred to as a register.

- Shift freq. = 25 MHz.
- Power dissipation = 195 mw
- These 4-bit registers feature parallel & serial inputs, parallel outputs, mode control, & 2 clock inputs.

The registers have 3 modes of operation:

1) Parallel (Broadside) load
2) Shift right (Q_A towards Q_D).
3) Shift left (Q_D towards Q_A).

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops & appears at the outputs after the high-to-low transition of the clock-2 input.

During loading, the entry of serial data is inhibited. The function table is shown here.

TABLE XVI. Function Table.

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2(L)	CLOCKS 1(R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_{BO}	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
L	X	↓	H	X	X	X	X	H	Q_{AN}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state),

X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level. a,b,c,d = the level of steady-state input at inputs A,B,C, or D, respectively. Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established. Q_{An},Q_{Bn},Q_{Cn}, Q_{Dn}= the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.